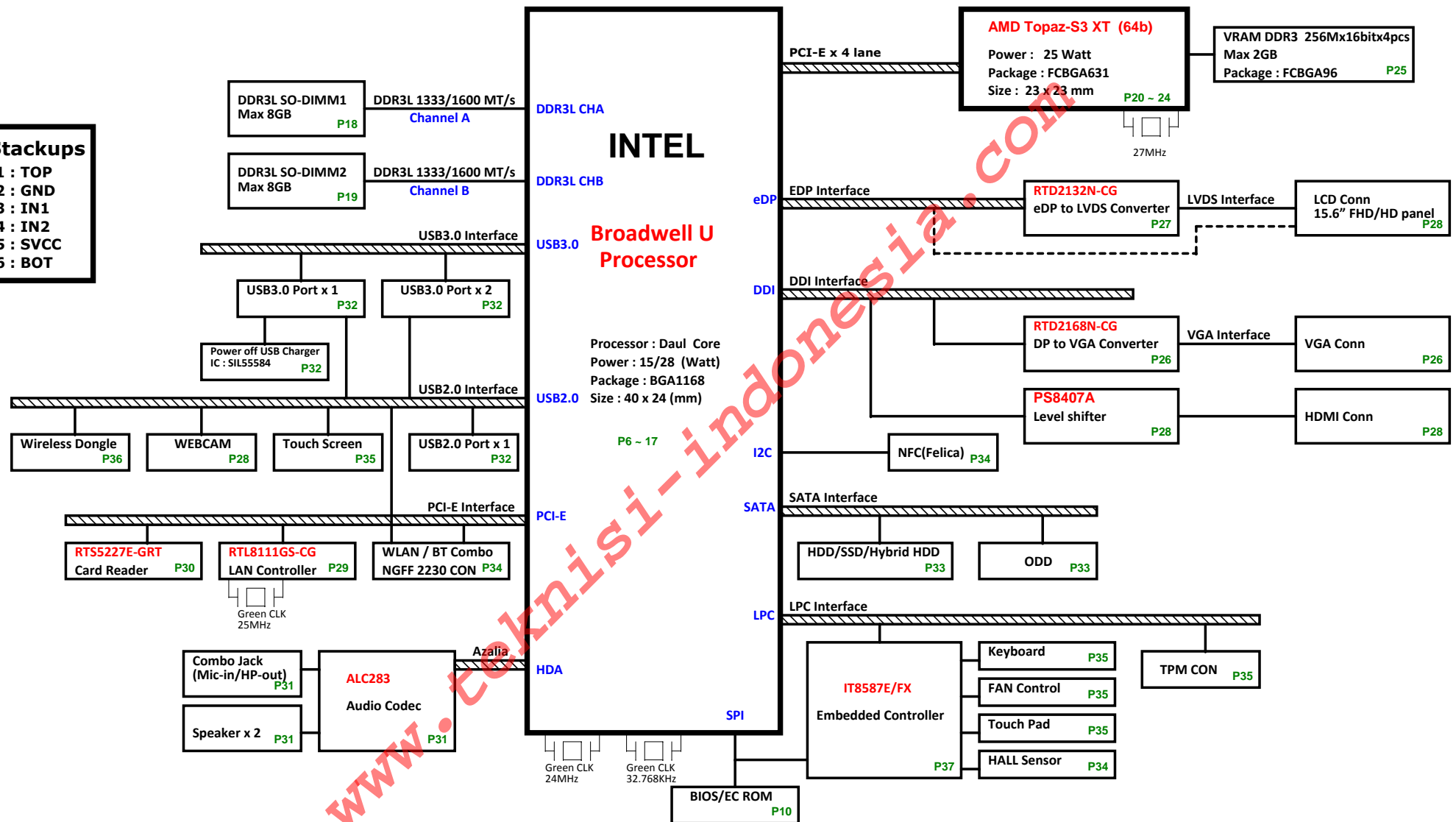


FH9 DIS (15.6") Broadwell Platform Block Diagram

PCB Stackups

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT



Quanta Computer Inc.

PROJECT : FH9

Size	Document Number	Rev
	BLOCK DIAGRAM	2A
Date:	Wednesday, November 19, 2014	Sheet 1 of 48

Table of Contents

PAGE	DESCRIPTION
01	Block Diagram
02	Front Page
03	Power Sequence
04	Clock Distribution
05	SMBus Address
06	BDW MCP(Display/eDP)
07	BDW MCP(Memory)
08	BDW PCH(GPIO/LPIO/MISC)
09	BDW PCH(PCIe/USB)
10	BDW PCH(RTC/HDA/SATA)
11	BDW PCH(CLK/LPC/SPI/SMB)
12	BDW PCH(Power management)
13	BDW MCP(Power)
14	BDW MCP(GND/DAISY/RSVD)
15	BDW MCP(CFG)
16	BDW PCH(Power)
17	BDW MCP(Sideband)
18	DDR3L DIMM-1-RVS(H4.0)
19	DDR3L DIMM-2-RVS(H4.0)
20	TOPAZ_S3_Pcie_Interface
21	TOPAZ_S3_Main/DP Power
22	TOPAZ_S3_GND/LVDS/Strap
23	TOPAZ_S3_Power
24	TOPAZ_S3_MEM_Interface
25	TOPAZ_S3_VRAM_DDR3 BGA96
26	DP to VGA (RTD2168)/CRT
27	eDP to LVDS (RTD2132N-CG)
28	HDMI/LVDS
29	LAN RTL8111GS/RJ45 conn
30	Card Reader (RTS5227E)
31	Audio ALC283
32	USB3.0/Charger/USB2.0
33	HDD/ODD/LED
34	WLAN/BT/ NFC/MMB/PWR
35	KB/FAN/TP/TPM/TS
36	G-CLK/WL Dongle/HOLE
37	EC_IT8587
38	VIN/CHARGER-ISL88732
39	SYSTEM 5V/3V(TPS51225RUK)
40	1.05V-GS335
41	DDR3L 1.35V(RT8231AGQW)
42	SWITCH
43	CPU_CORE(NCP81101B) 28W
44	VGA CORE(INTERISL 62771)
45	1.5GPU/0.95_GPU(RT8068A)
46	1.8V_GPU&3V_GPU
47	PWR Delivery/RESET/PWROK
48	Change History

Voltage Rails

Power	Voltage	S0	S3	S4	S5	G3	Ctl Signal
3V_RTC	3V	ON	ON	ON	ON	ON	
VIN	19V	ON	ON	ON	ON	OFF	Adaptor in
5V_AUX	5V	ON	ON	ON	ON	OFF	Adaptor in
3V_AUX	3.3V	ON	ON	ON	ON	OFF	Adaptor in
5V_S5	5V	ON	ON	ON	ON	OFF	S5_ON
3V_S5	3.3V	ON	ON	ON	ON	OFF	S5_ON
1.35V_S3	1.35V	ON	ON	OFF	OFF	OFF	S3_ON
5V_S3	5V	ON	ON	OFF	OFF	OFF	S3_ON
3VDUAL_LAN	3.3V	ON	OFF	OFF	OFF	OFF	LAN_ON_EC
3V_WLAN	3.3V	ON	OFF	OFF	OFF	OFF	WLAN_ON
5V_S0	5V	ON	OFF	OFF	OFF	OFF	S0_ON_1
3V_S0	3.3V	ON	OFF	OFF	OFF	OFF	S0_ON_2
1.5V_S0	1.5V	ON	OFF	OFF	OFF	OFF	S0_ON_3
1.05V_S0	1.05V	ON	OFF	OFF	OFF	OFF	S0_ON_1
1.05V_VCCST	1.05V	ON	OFF	OFF	OFF	OFF	S0_ON_1
DDR_VTERM	0.675V	ON	OFF	OFF	OFF	OFF	DDR_PG
VCC_CORE	1.7V	ON	OFF	OFF	OFF	OFF	H_VR_EN_MCP
VGA_CORE	1V	ON	OFF	OFF	OFF	OFF	1.8VGPU_PG
3V_GPU	3.3V	ON	OFF	OFF	OFF	OFF	GPU_ON
1.8V_GPU	1.8V	ON	OFF	OFF	OFF	OFF	GPU_ON
1.5V_GPU	1.5V	ON	OFF	OFF	OFF	OFF	1.8VGPU_PG
0.95V_GPU	0.95V	ON	OFF	OFF	OFF	OFF	GPU_ON

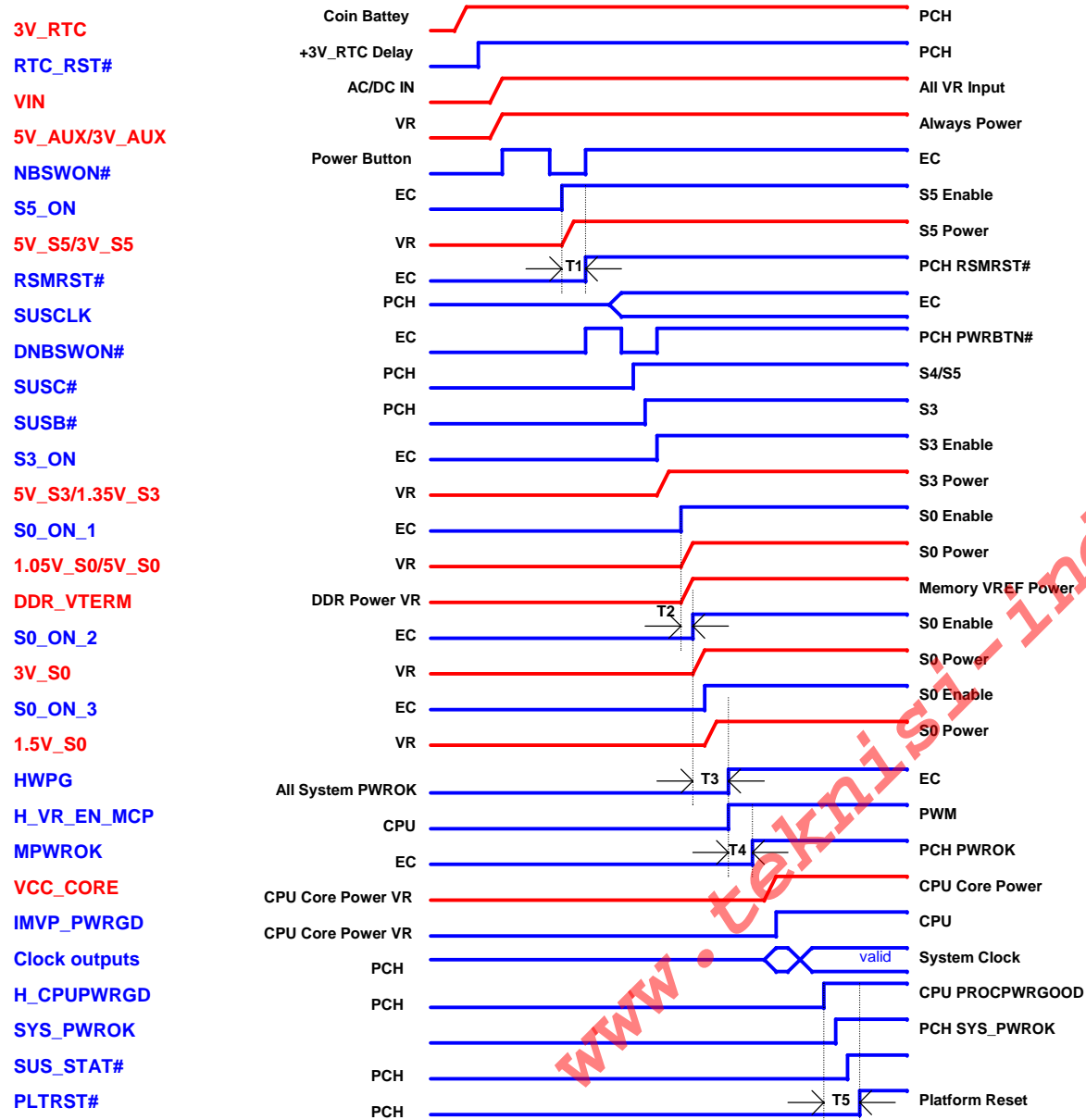
Function List

USB2		PCIE		Display		USB3		SATA	
Port 0	Co-lay USB3.0	Port 1	Card Reader	eDP Port 1	LVDS or eDP	Port 1	USB3.0 Conn	Port 0	HDD
Port 1	Co-lay USB3.0	Port 2	USB3.0 Conn	eDP Port 2	NC	Port 2	USB3.0 Conn	Port 1	ODD
Port 2	Co-lay USB3.0	Port 3	WLAN	DDI Port 1	HDMI	Port 3	Card Reader	Port 2	NC
Port 3	Touch screen	Port 4	GLAN	DDI Port 2	CRT	Port 4	USB3.0 Conn	Port 3	NC
Port 4	Camera	Port 5	GPU(TOPAZ)						
Port 5	USB2.0 Conn								
Port 6	Bluetooth								
Port 7	USB HUB								

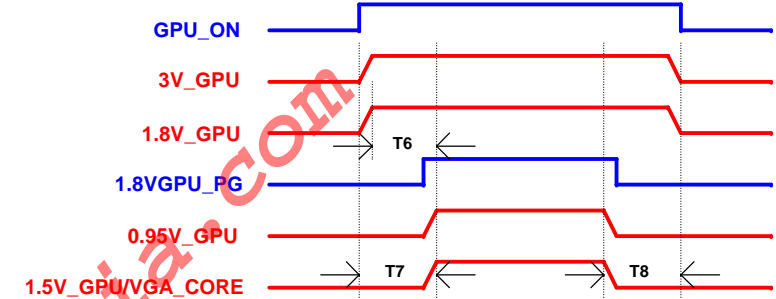
Function Select

S@	TOPAZ + VRAM
L@	RTD2132N-CG
E@	Internal eDP
V@	RTD2168
N@	NFC
M@	MMB
TS@	Touch screen
WL@	Wireless Dongle

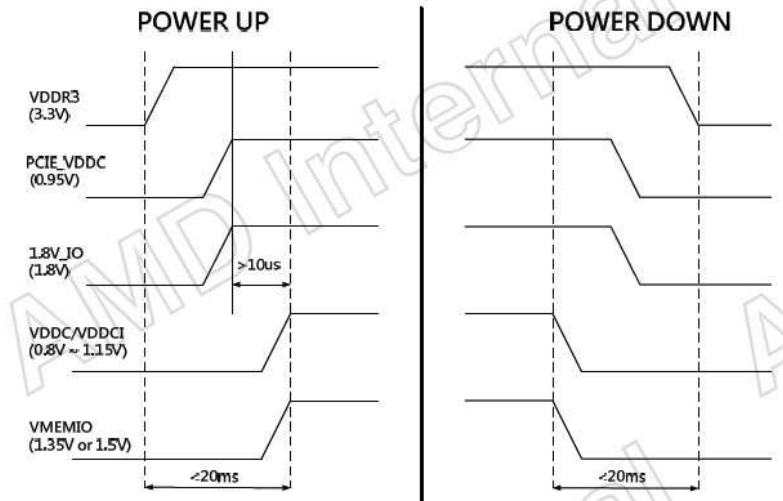
System Power On Sequencing Timing Diagram

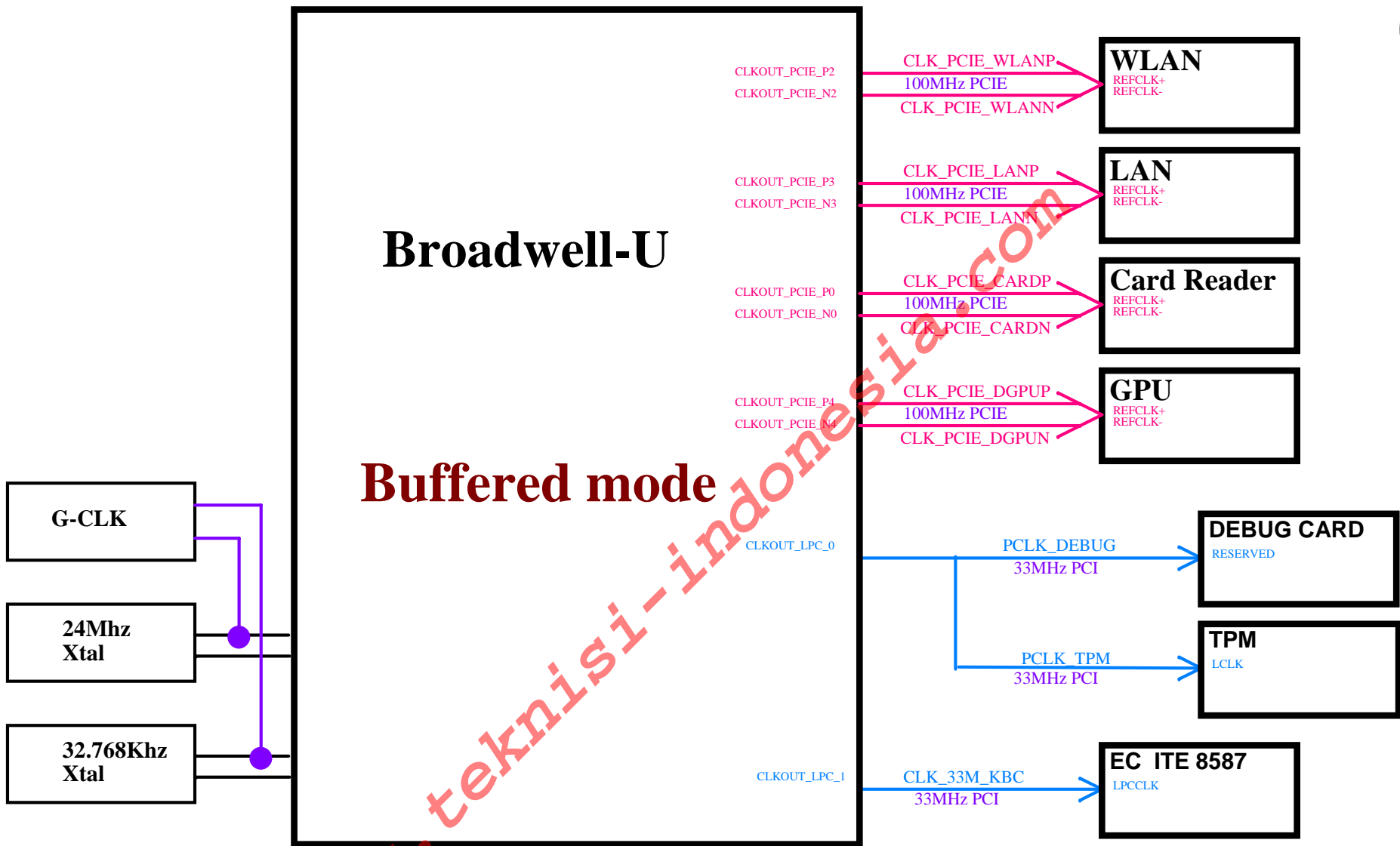


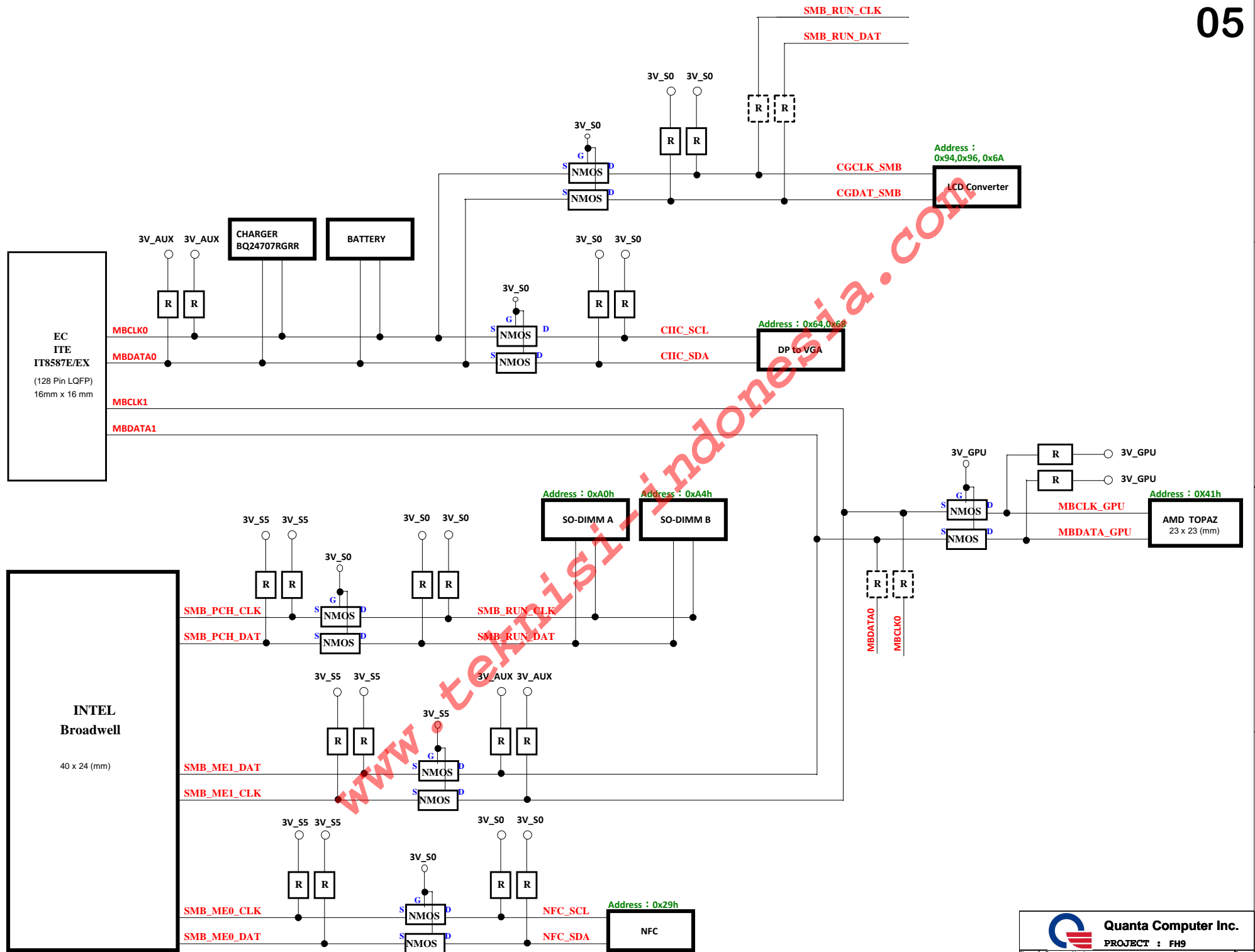
dGPU Power On/Off Sequencing Timing Diagram



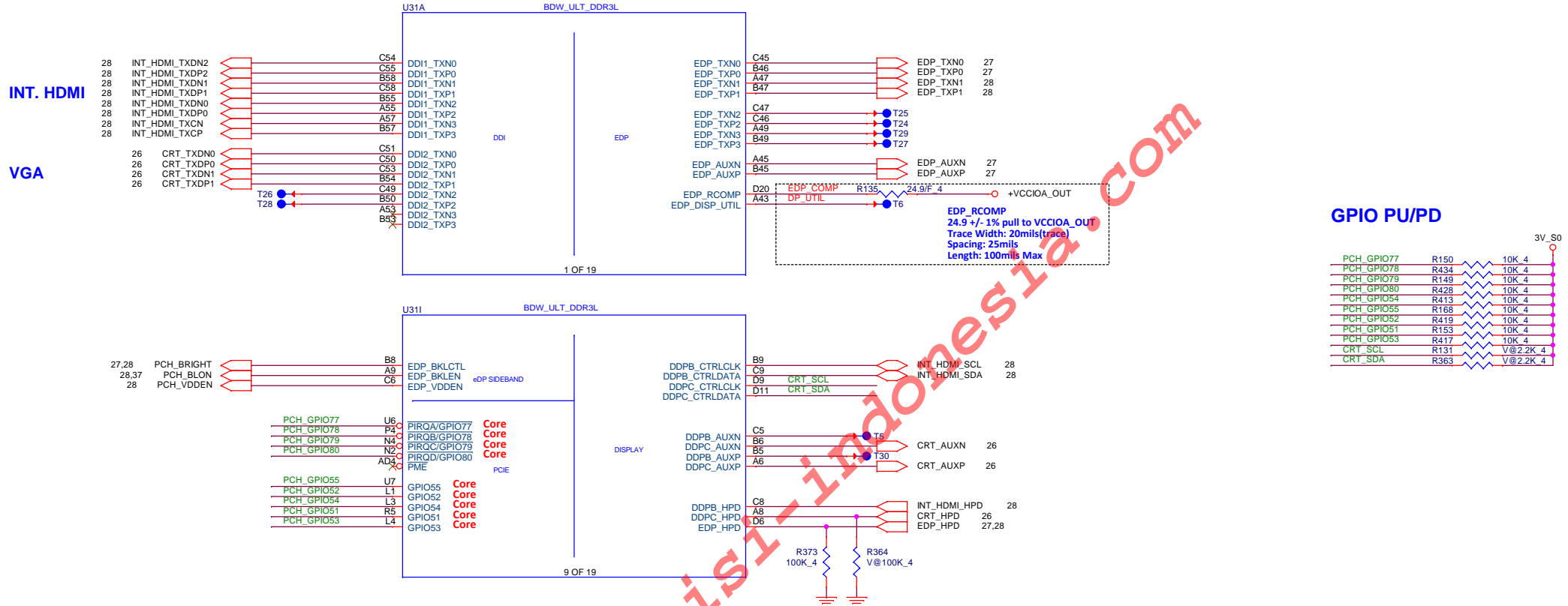
POWER UP / POWER DOWN SEQUENCE

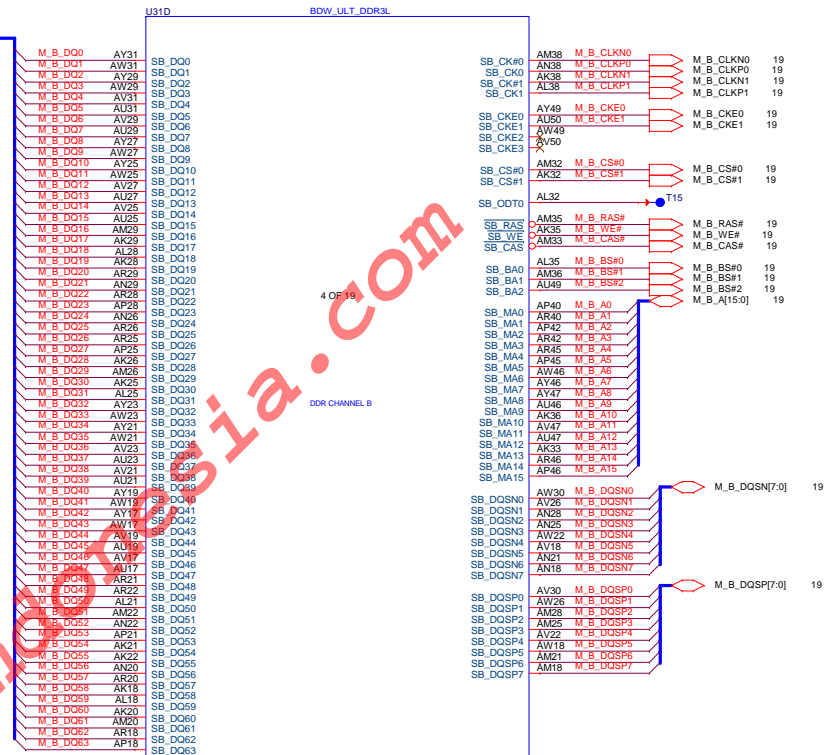
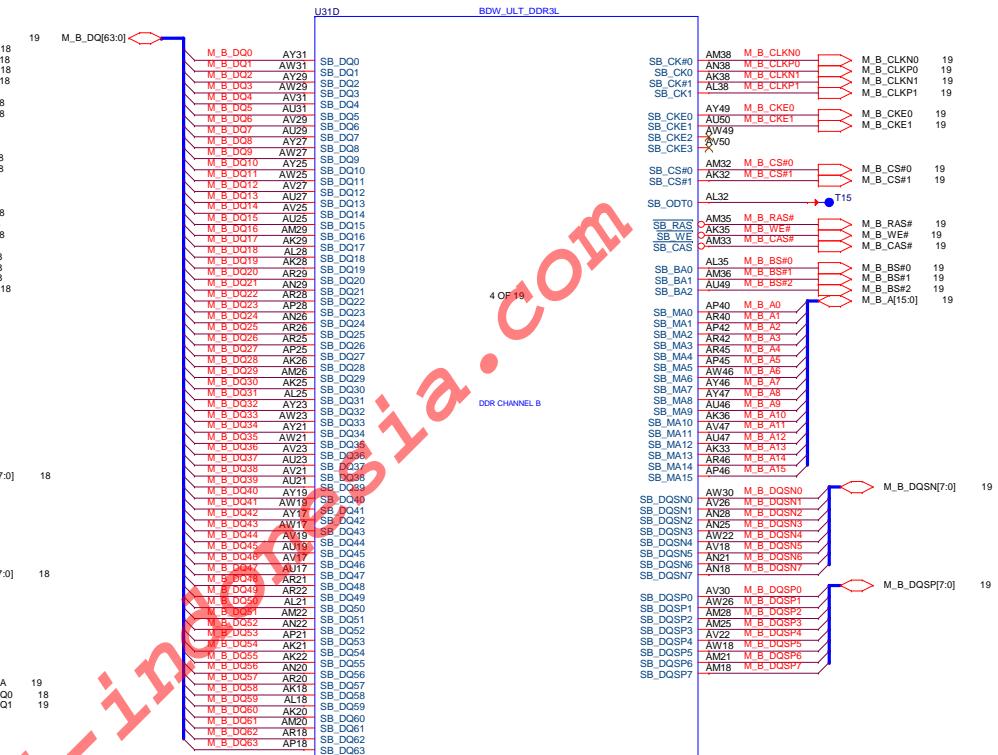






Broadwell Type-U ULT (DISPLAY)





Broadwell Type-U ULT (GPIO, LPIO, MISC)

GPIO27

With Intel LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from DSx

For GPU use

37,44,45 GPU_PWRGD

For GPU use

20,37 GPU_RST#_PCH

37 SIO_EXT_SMI#

37 SIO_EXT_SCI#

SIO_EXT_SMI# R583

SIO_EXT_SCI# R584

B-34

33 DEVSLP0

34 NFC_DWL_REQ

10,31 ACZ_SPKR

C283

*100P/50V_4

P1

P2

P3

P4

P5

P6

P7

P8

P9

P10

P11

P12

P13

P14

P15

P16

P17

P18

P19

P20

P21

P22

P23

P24

P25

P26

P27

P28

P29

P30

P31

P32

P33

P34

P35

P36

P37

P38

P39

P40

P41

P42

P43

P44

P45

P46

P47

P48

P49

P50

P51

P52

P53

P54

P55

P56

P57

P58

P59

P60

P61

P62

P63

P64

P65

P66

P67

P68

P69

P70

P71

P72

P73

P74

P75

P76

P77

P78

P79

P80

P81

P82

P83

P84

P85

P86

P87

P88

P89

P90

P91

P92

P93

P94

P95

P96

P97

P98

P99

P100

P101

P102

P103

P104

P105

P106

P107

P108

P109

P110

P111

P112

P113

P114

P115

P116

P117

P118

P119

P120

P121

P122

P123

P124

P125

P126

P127

P128

P129

P130

P131

P132

P133

P134

P135

P136

P137

P138

P139

P140

P141

P142

P143

P144

P145

P146

P147

P148

P149

P150

P151

P152

P153

P154

P155

P156

P157

P158

P159

P160

P161

P162

P163

P164

P165

P166

P167

P168

P169

P170

P171

P172

P173

P174

P175

P176

P177

P178

P179

P180

P181

P182

P183

P184

P185

P186

P187

P188

P189

P190

P191

P192

P193

P194

P195

P196

P197

P198

P199

P200

P201

P202

P203

P204

P205

P206

P207

P208

P209

P210

P211

P212

P213

P214

P215

P216

P217

P218

P219

P220

P221

P222

P223

P224

P225

P226

P227

P228

P229

P230

P231

P232

P233

P234

P235

P236

P237

P238

P239

P240

P241

P242

P243

P244

P245

P246

P247

P248

P249

P250

P251

P252

P253

P254

P255

P256

P257

P258

P259

P260

P261

P262

P263

P264

P265

P266

P267

P268

P269

P270

P271

P272

P273

P274

P275

P276

P277

P278

P279

P280

P281

P282

P283

P284

P285

P286

P287

P288

P289

P290

P291

P292

P293

P294

P295

P296

P297

P298

P299

P300

P301

P302

P303

P304

P305

P306

P307

P308

P309

P310

P311

P312

P313

P314

P315

P316

P317

P318

P319

P320

P321

P322

P323

P324

P325

P326

P327

P328

P329

P330

P331

P332

P333

P334

P335

P336

P337

P338

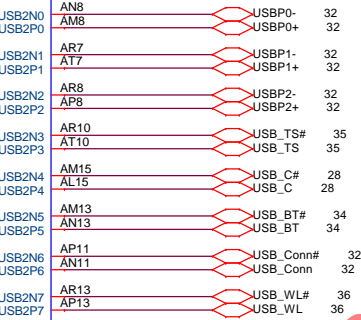
P339

For GPU use

U31K

BDW_ULT_DDR3L

USB debug port



USB2.0 Port (Co-lay USB3.0)

USB2.0 Port (Co-lay USB3.0)

USB2.0 Port (Co-lay USB3.0)

Touch screen

Camera

Bluetooth

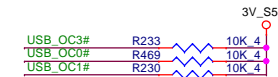
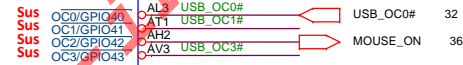
USB2.0 Port

Wireless Dongle

USB3.0

USB3.0

USBBIAS & USBBIAS#
Short the USBBIAS and the USBBIAS# pins and one end of 22.6 +/- 1% to GND
Route signal using 50 ohm single-ended impedance
Spacing: 15mils
Length: 500mils Max



TOPAZ

WLAN(NGFF)

GLAN

Card Reader

USB3.0

PCIE_RCOMP
3K+/- 1% pull to VCCUSB3PLL
Trace Width: 12-15mils(trace)
Spacing: 12mils
Length: 500mils Max

PCIE_IREF
Directly connect to VCCUSB3PLL
Trace Width: 12-15mils(trace)
Spacing: 12mils
Length: 500mils Max

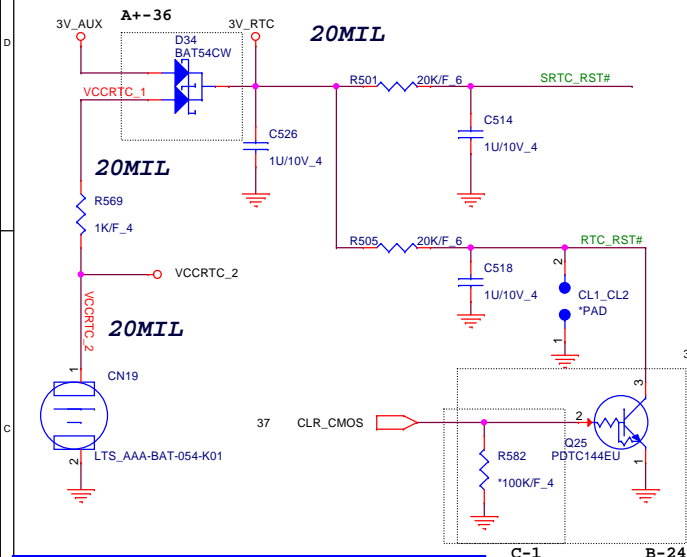
www.teknisi.id



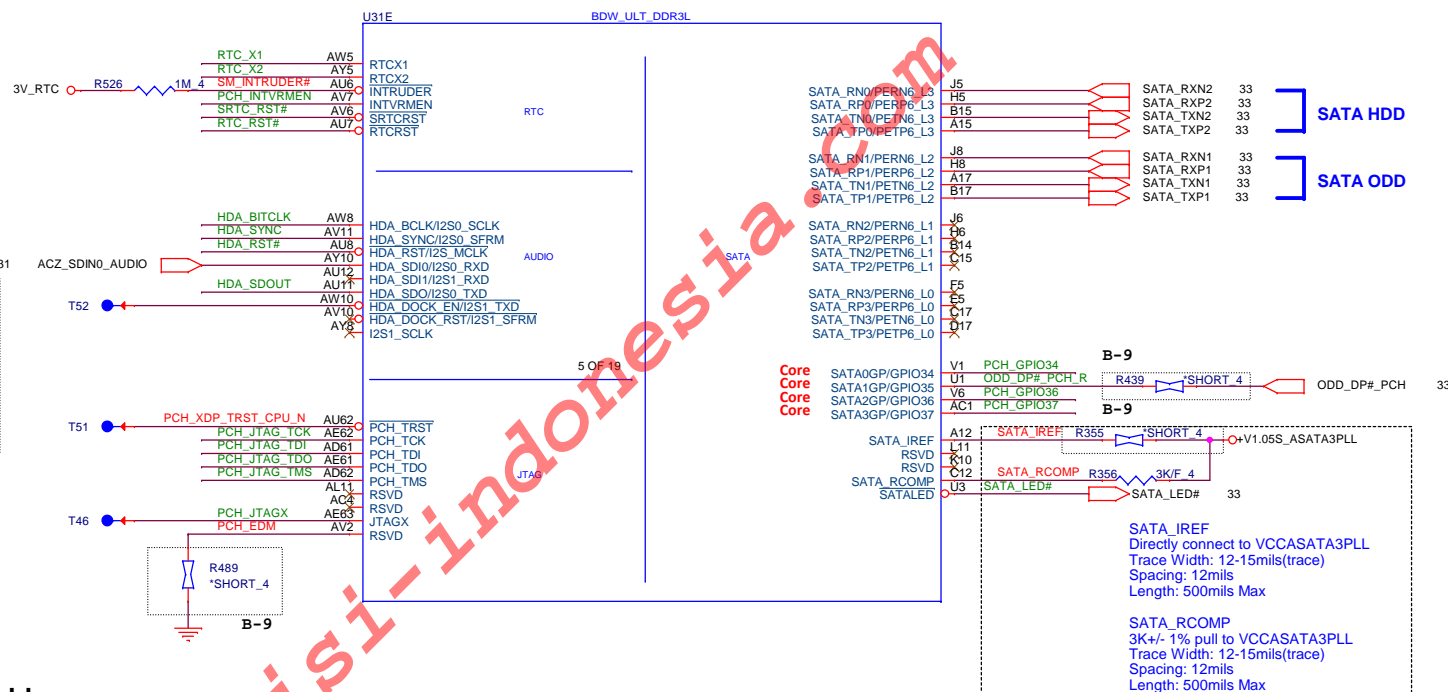
Quanta Computer Inc.

PROJECT : FH9

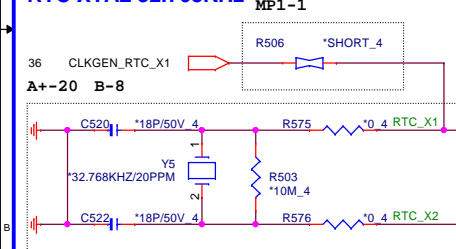
RTC Circuitry(RTC)



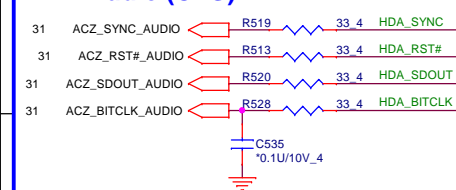
Broadwell Type-U ULT (RTC,HDA,JTAG,SATA)



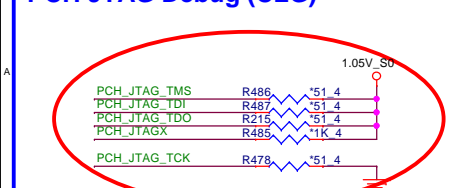
RTC XTAL 32.768KHz



HDA Audio (CLG)



PCH JTAG Debug (CLG)

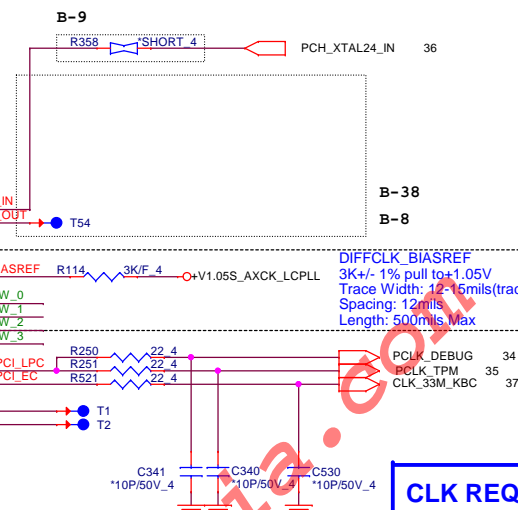
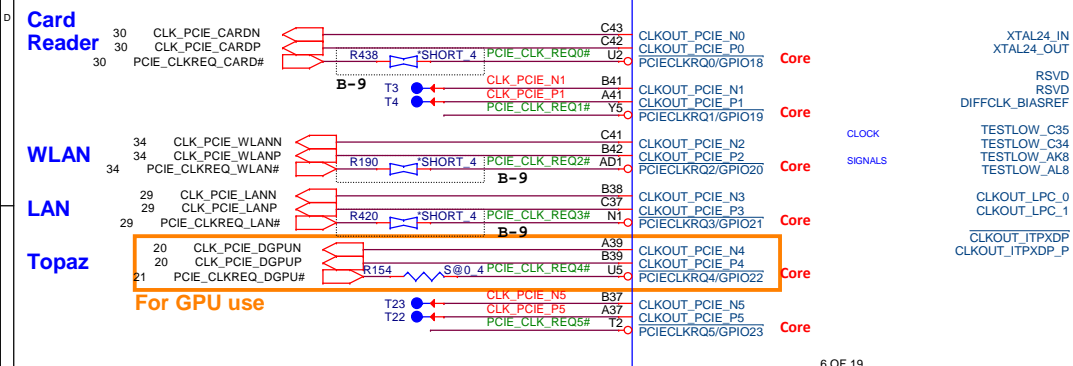


PCH Strap Table

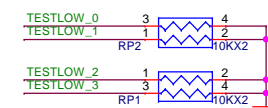
Pin Name	Strap description	Sampled	Configuration	Schematic
HDA_SDO/I2S0_TXD	Flash Descriptor Security Override	PWROK	0 = Enable Flash Descriptor security. (Int PD) 1 = Disable Flash Descriptor Security	3V_S5 - R518 - *1K_4 - HDA_SDOOUT 37
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	0 = DCPSUSx are powered from an ext. power source 1 = Integrated VRM enabled (330K PU VccRTC)	3V_RTC - R515 - 330K_4 - PCH_INTVRMEN - R517 - *330K_4
DSWVRMEN	DeepSx Well On-Die VRM Enable	ALWAYS	0 = Disable Integrated DSW On-Die VRM 1 = Enable Integrated DSW On-Die VRM (Must be PU)	3V_RTC - R514 - 330K_4 - DSWVRMEN 12
GPIO15	TLS Confidentiality	RSMRST#	0 = Disable Intel ME Crypto TLS cipher suite (Int PD) 1 = Enable Intel ME Crypto Transport	8 PCH_GPIO15 - R197 - 8.2K_4 - R200 - *1K_4
SPKR/GPIO81	No reboot mode setting	PWROK	0 = Disable No Reboot mode (Int PD). 1 = Enable No Reboot mode.	3V_S0 - R181 - *1K_4 - ACZ_SPKR 8,31
GSPIO_MOS/GPIO86	Boot BIOS Strap Bit	PWROK	0 = Boot from SPI 1 = Boot from LPC	3V_S0 - R392 - *1K_4 - R396 - *1K_4 - BBS 8
SDIO_D0/GPIO66	Top Swap Override	PWROK	0 = Disable Top Swap mode. (Int PD) 1 = Enable Top Swap mode.	+V3.3S_1.8S_LPSS_SDIO - R391 - *1K_4 - R389 - *1K_4 - PCH_GPIO66 8

Quanta Computer Inc.
PROJECT : FH9

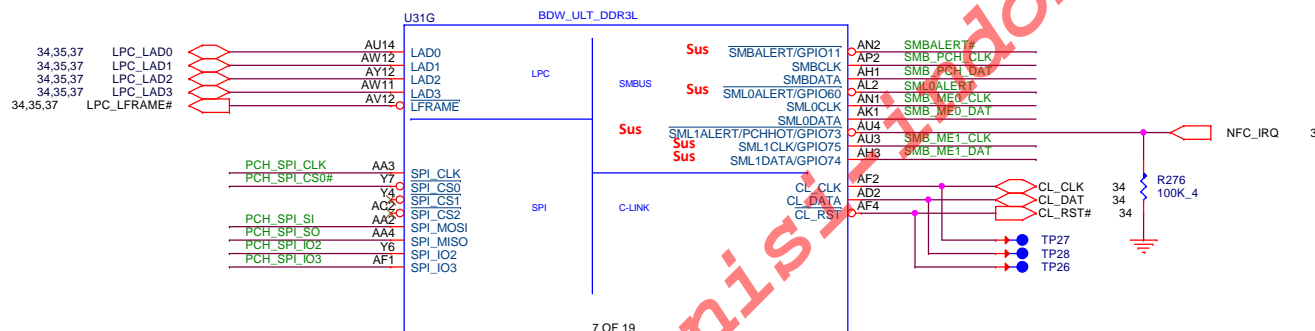
Broadwell Type-U ULT (CLK)



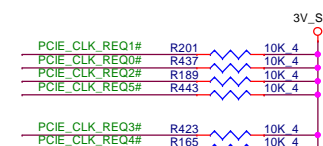
Do not short
the testlow pins together



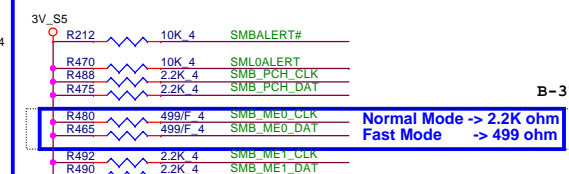
Broadwell Type-U ULT (LPC/SPI/SMB/CLINK)



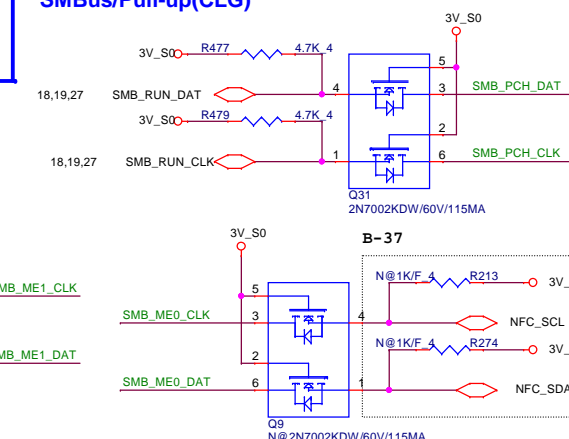
CLK REQ PU (CLG)



SMBus

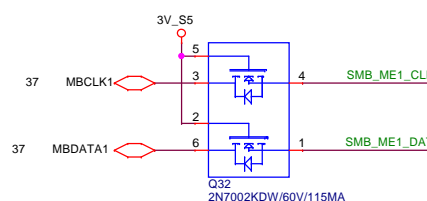
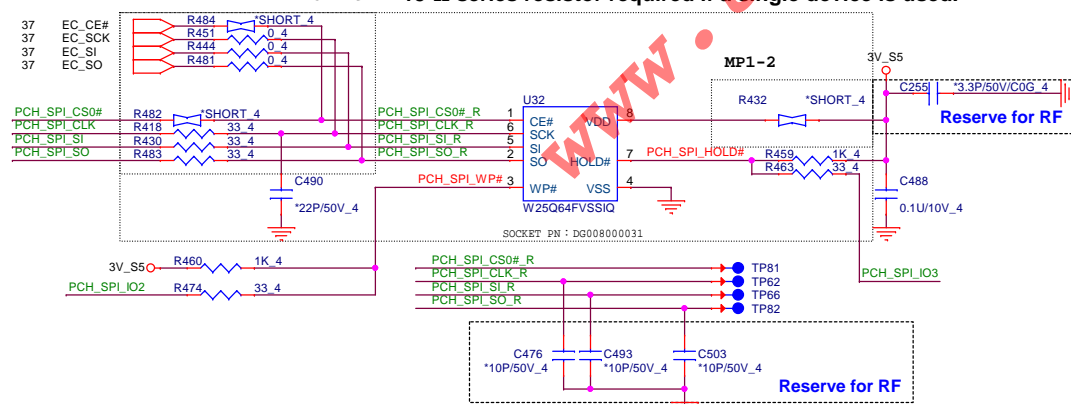


SMBus/Pull-up(CLG)



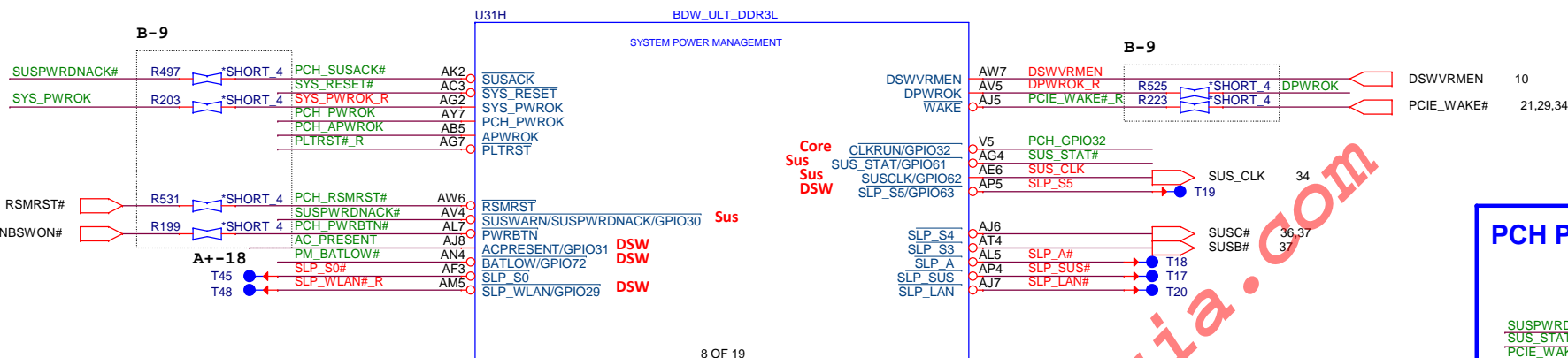
PCH Dual SPI
EC & BIOS & ME F/W ROM 8MB

Use one 33- Ω series-resistor per device if using two SPI devices. 15- Ω series resistor required if a single device is used.

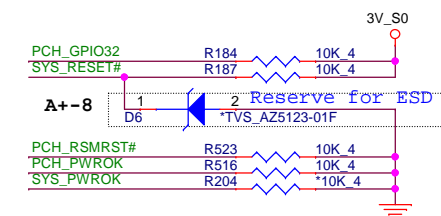
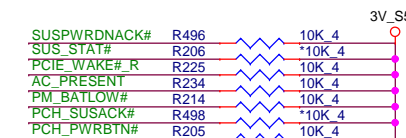


Broadwell U-Type ULT (SYSTEM POWER MANAGEMENT)

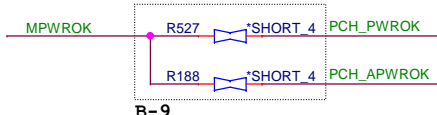
12



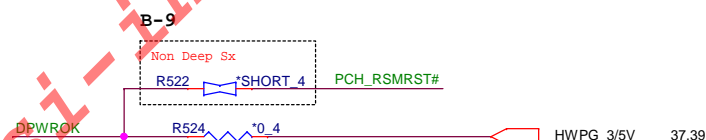
PCH PU/PD (CLG)



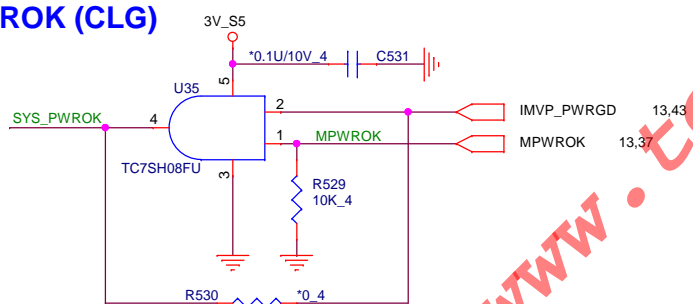
PCH PWROK (CLG)



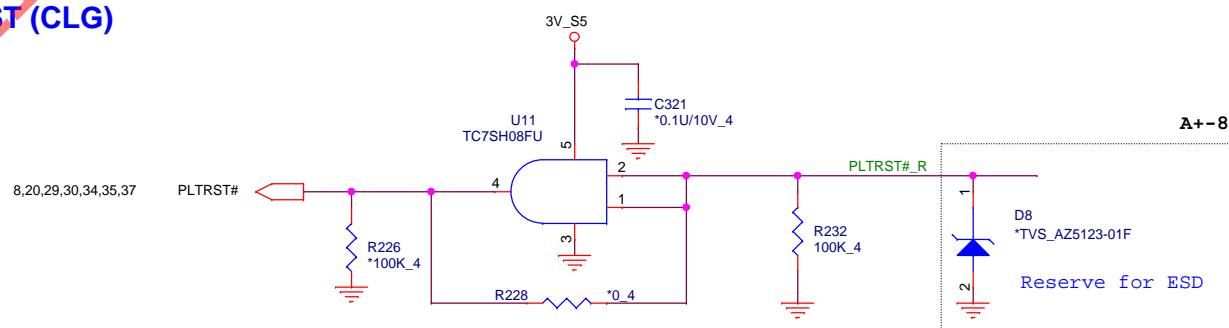
DSW Circuit



SUS PWROK (CLG)



PLTRST (CLG)



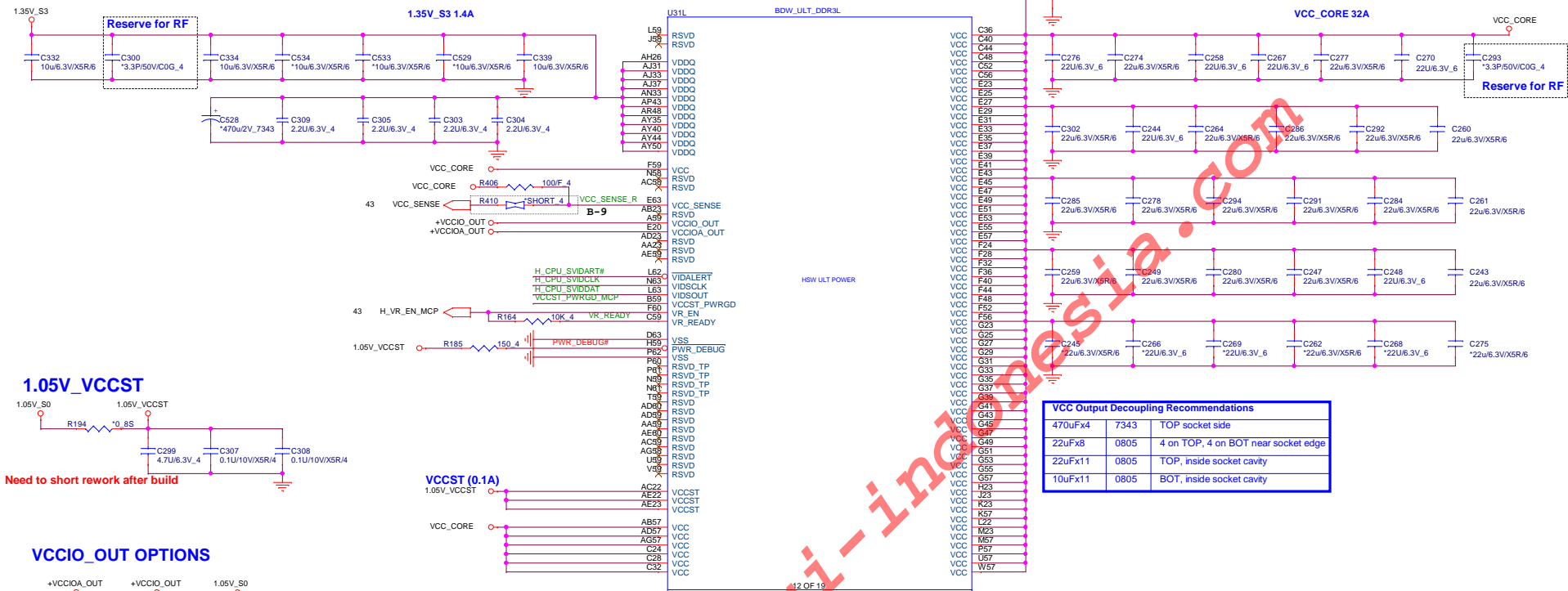
Quanta Computer Inc.

PROJECT : FH9

Size	Document Number	Rev 2A
BDW PCH(PWR MANAGEMENT)		
Date:	Wednesday, November 19, 2014	Sheet 12 of 48

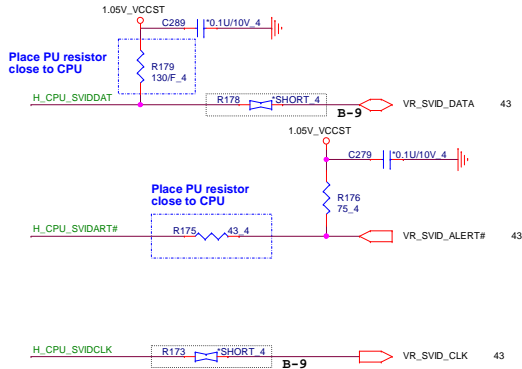
VDDQ Output Decoupling Recommendations			
330uFx2	7343	BOT socket side	
22uFx11	0805	5 on TOP, 6 on BOT inside socket cavity	
10uFx10	0805	5 on TOP, 5 on BOT inside socket cavity	

Broadwell U-Type ULT MCP(POWER)

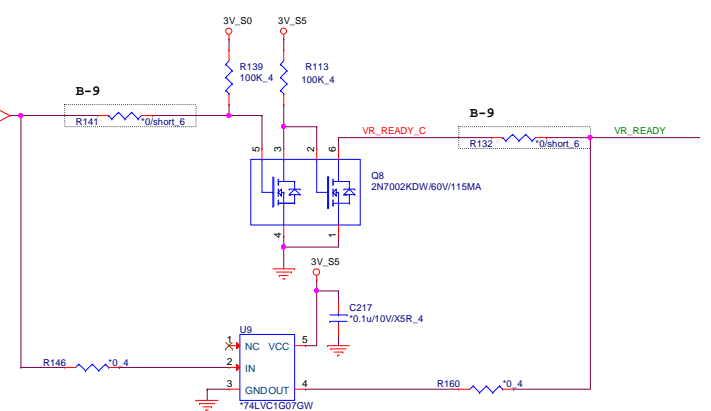
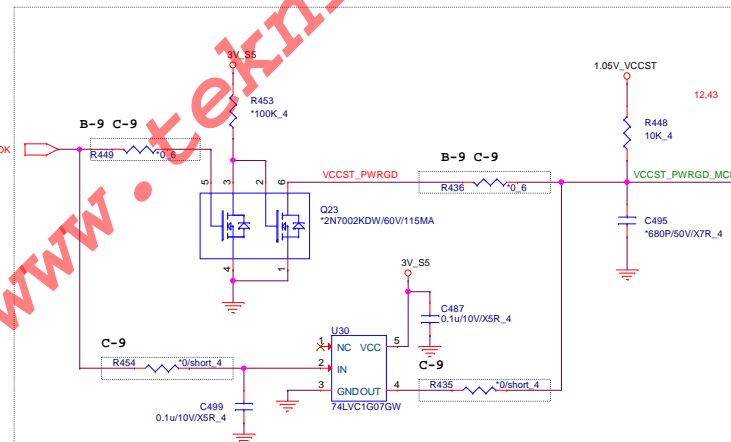


SVID

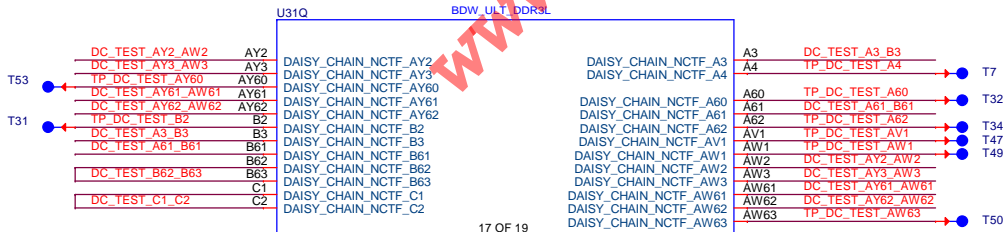
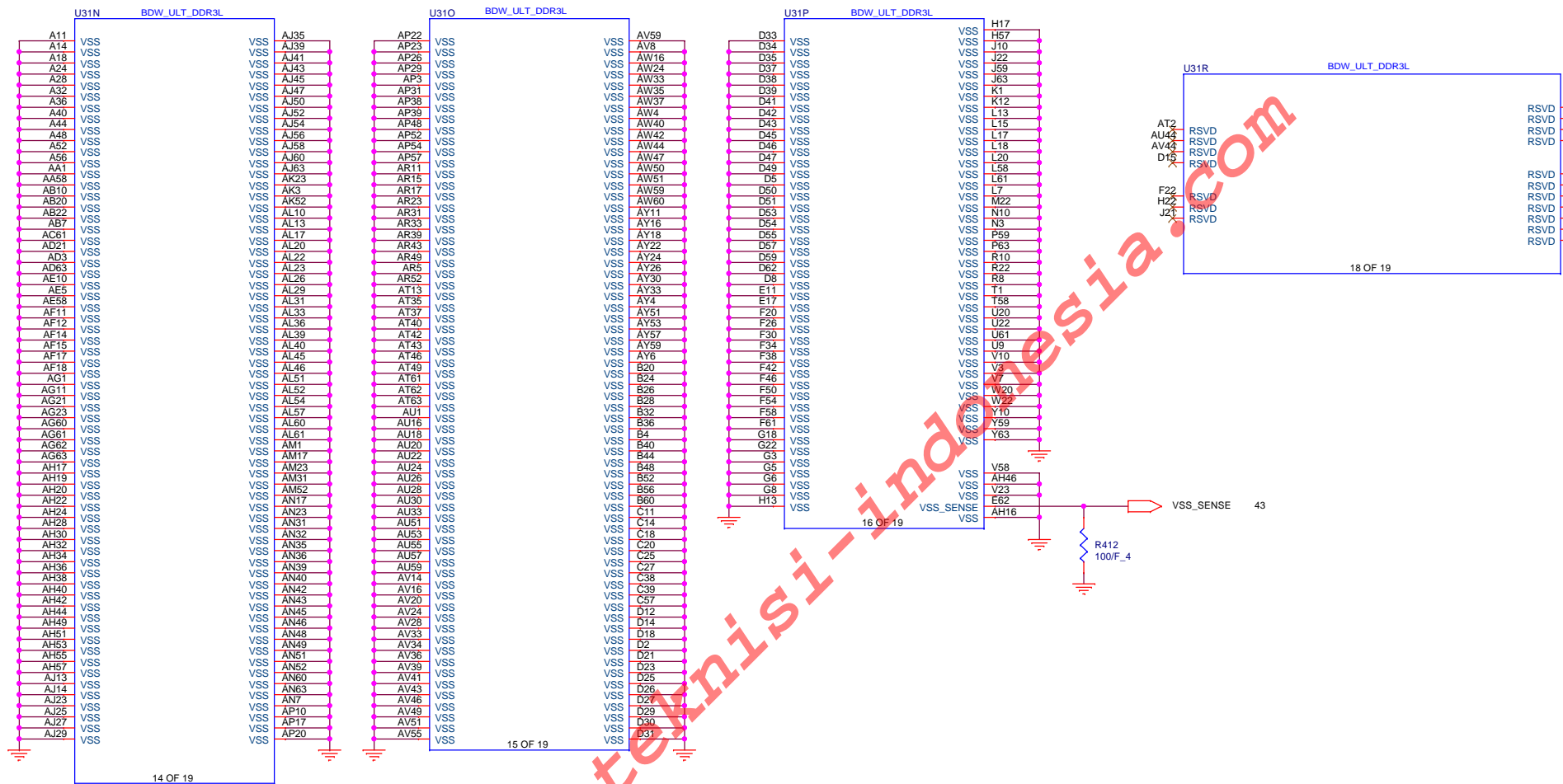
Layout note: need routing together and ALERT need between CLK and DATA.



B-68



Broadwell U-Type ULT (RSVD,GND)

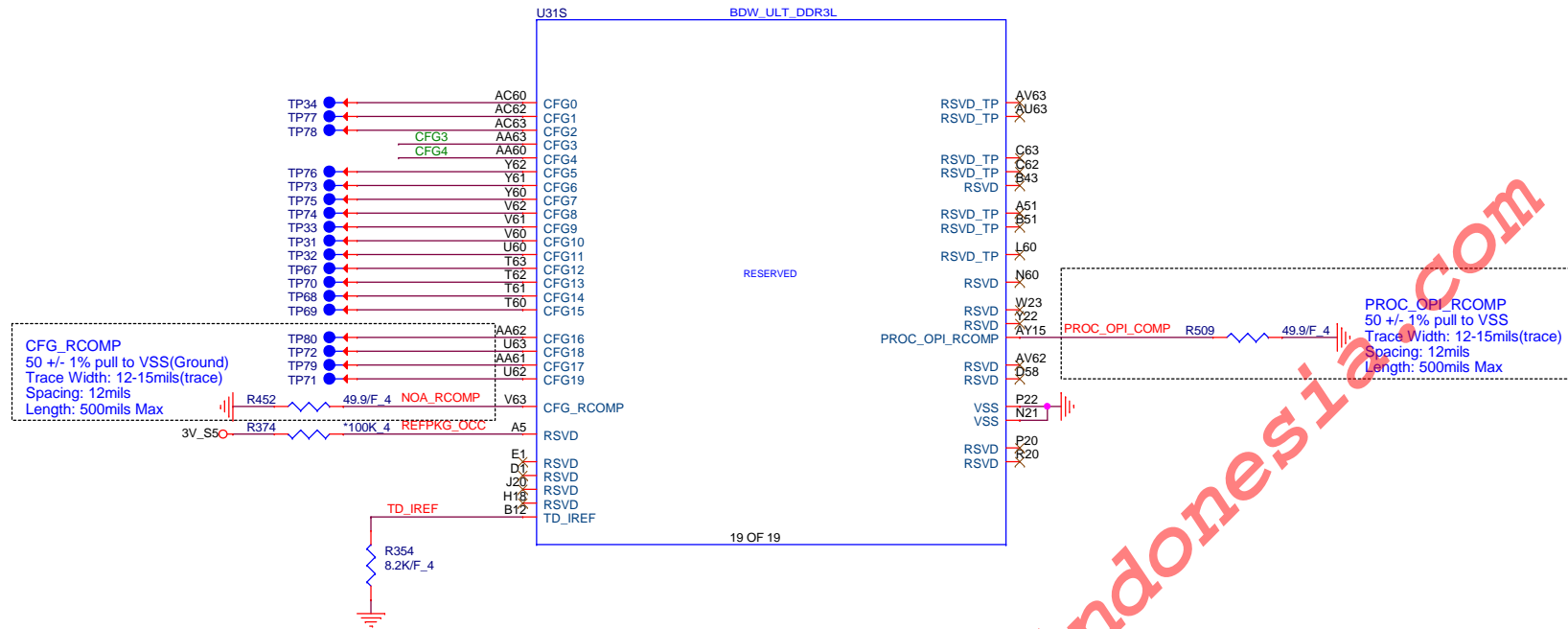


Quanta Computer Inc.



PROJECT : FH9

Size	Document Number	Rev
	BDW MCP(GND/DAISY/RSVD)	2A
Date:	Wednesday, November 19, 2014	Sheet 14 of 48

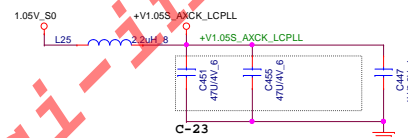
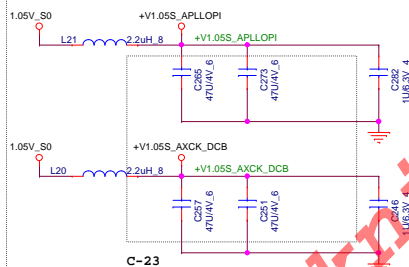
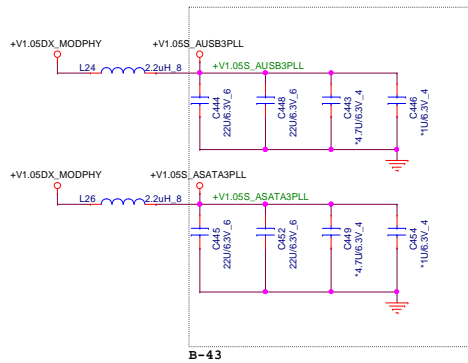
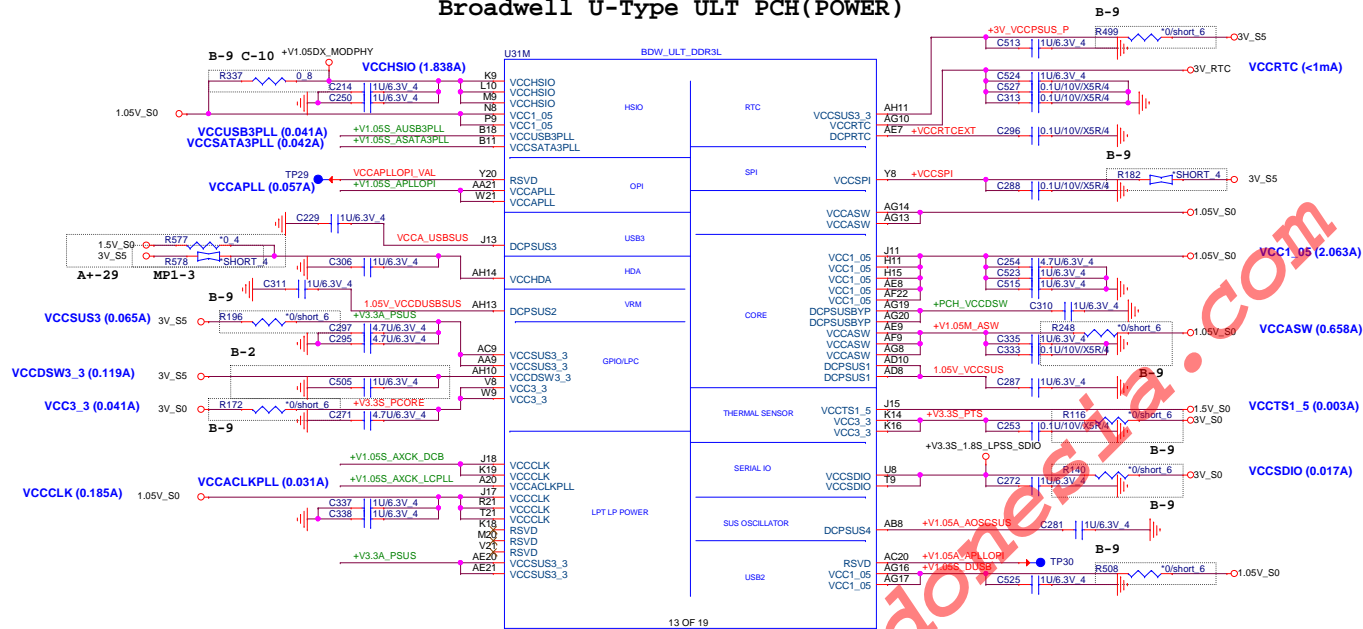
Broadwell U-Type ULT PCH (CFG)



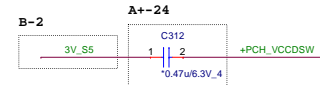
Processor Strapping

	1	0	
CFG3 MSR Privacy Bit Feature	Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting	IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden	
CFG4 eDP Enable	DISABLED	ENABLED	

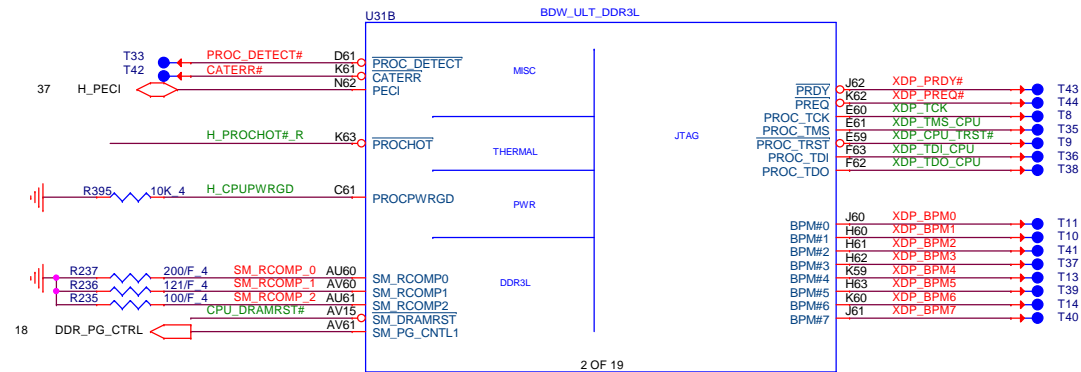
Broadwell U-Type ULT PCH(POWER)



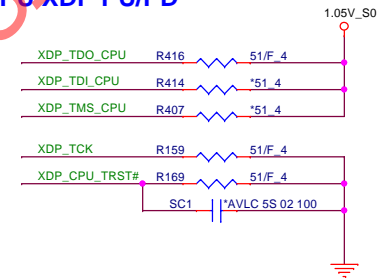
WW15 4/10 Intel VCCDSW3
G3 can't boot issue.



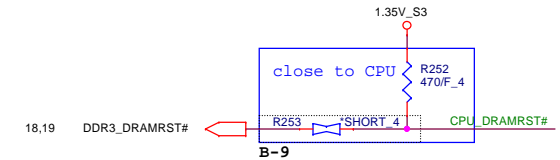
Broadwell U-Type ULT MCP(SIDEBAND)



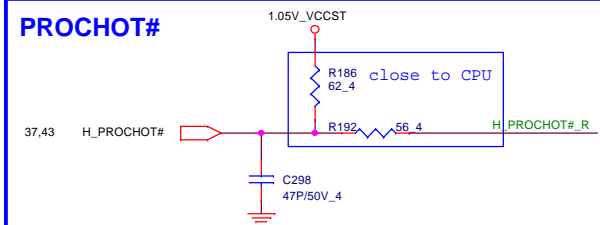
CPU_XDP PU/PD



SM_DRAMRST#

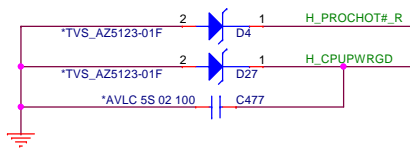


PROCHOT#



A+-8

Reserve for ESD



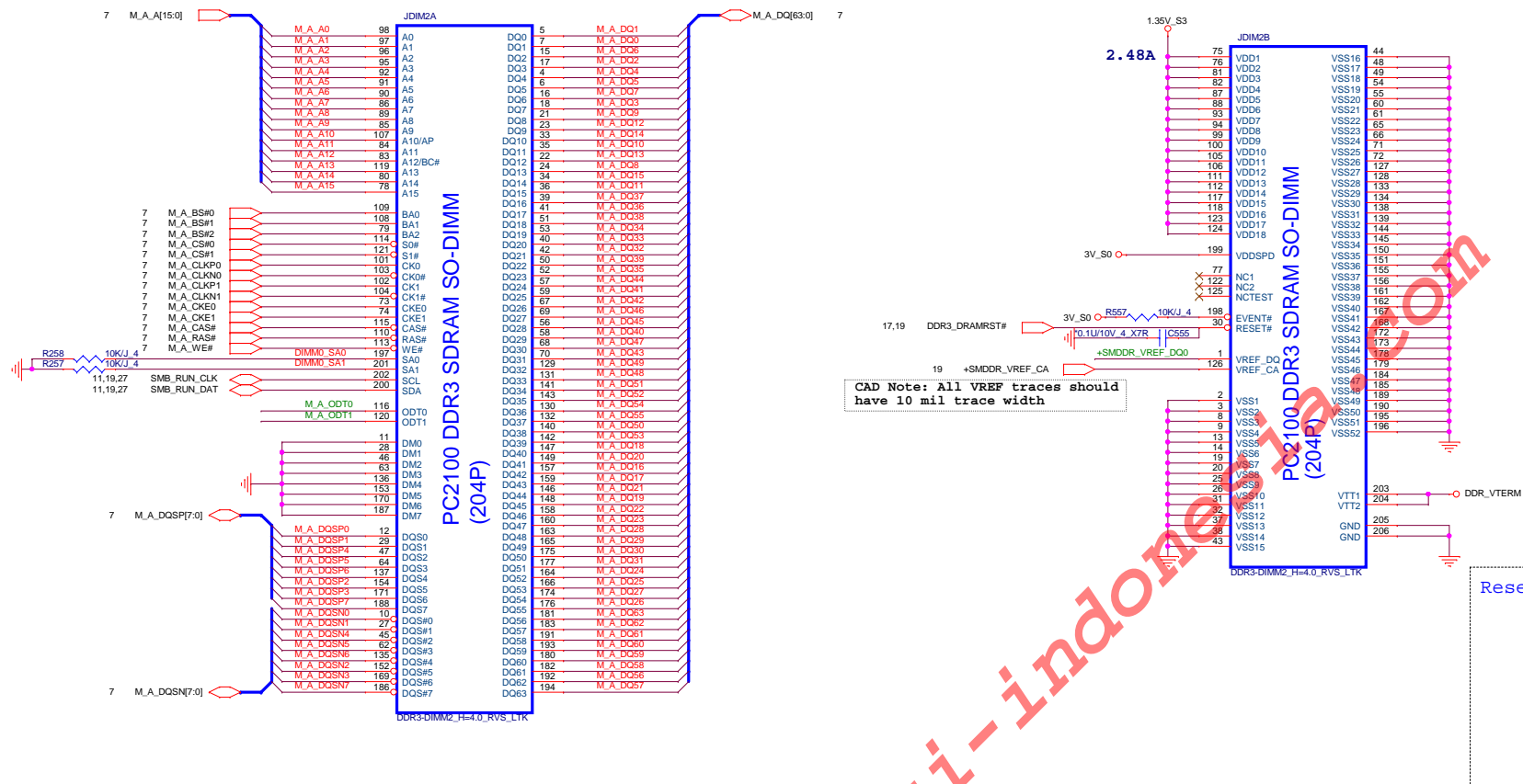
www.teknisi-indonesia.com



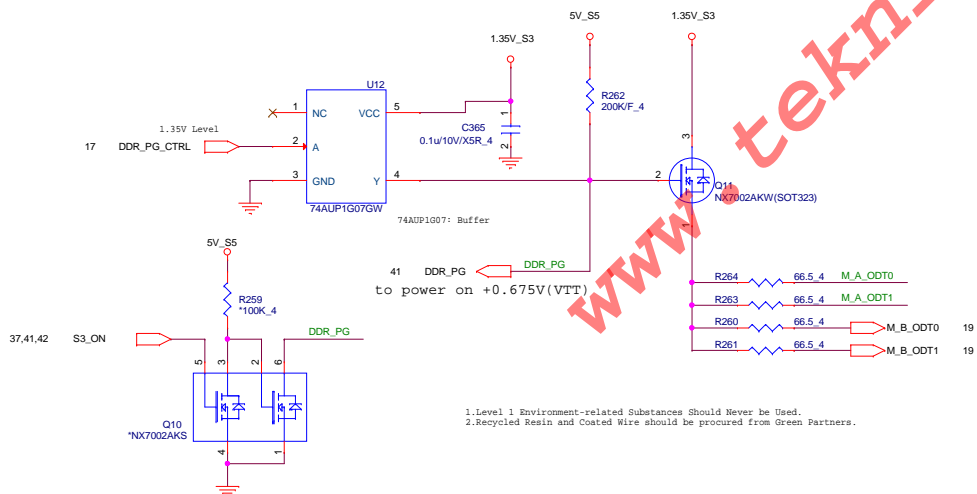
Quanta Computer Inc.

PROJECT : FH9

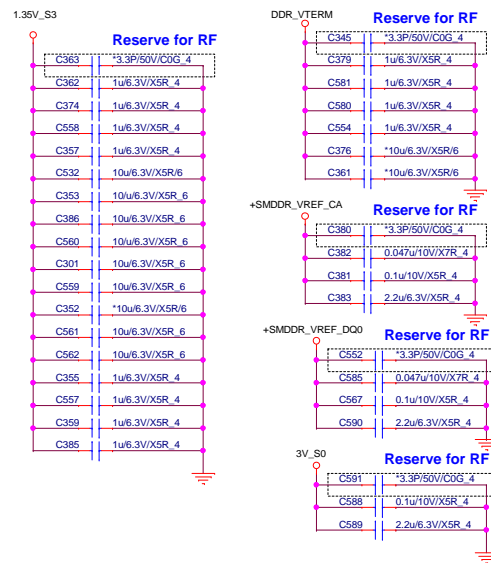
Size	Document Number	Rev
	BDW MCP(SIDEBAND)	2A
Date:	Wednesday, November 19, 2014	Sheet 17 of 48



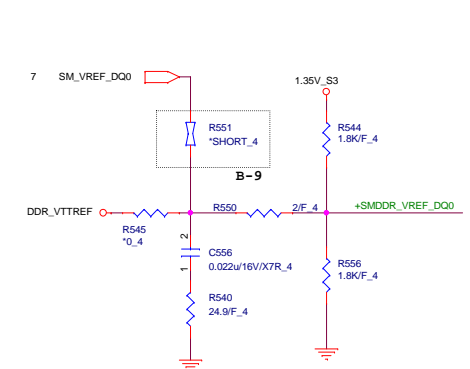
DDR3L SODIMM ODT GENERATION



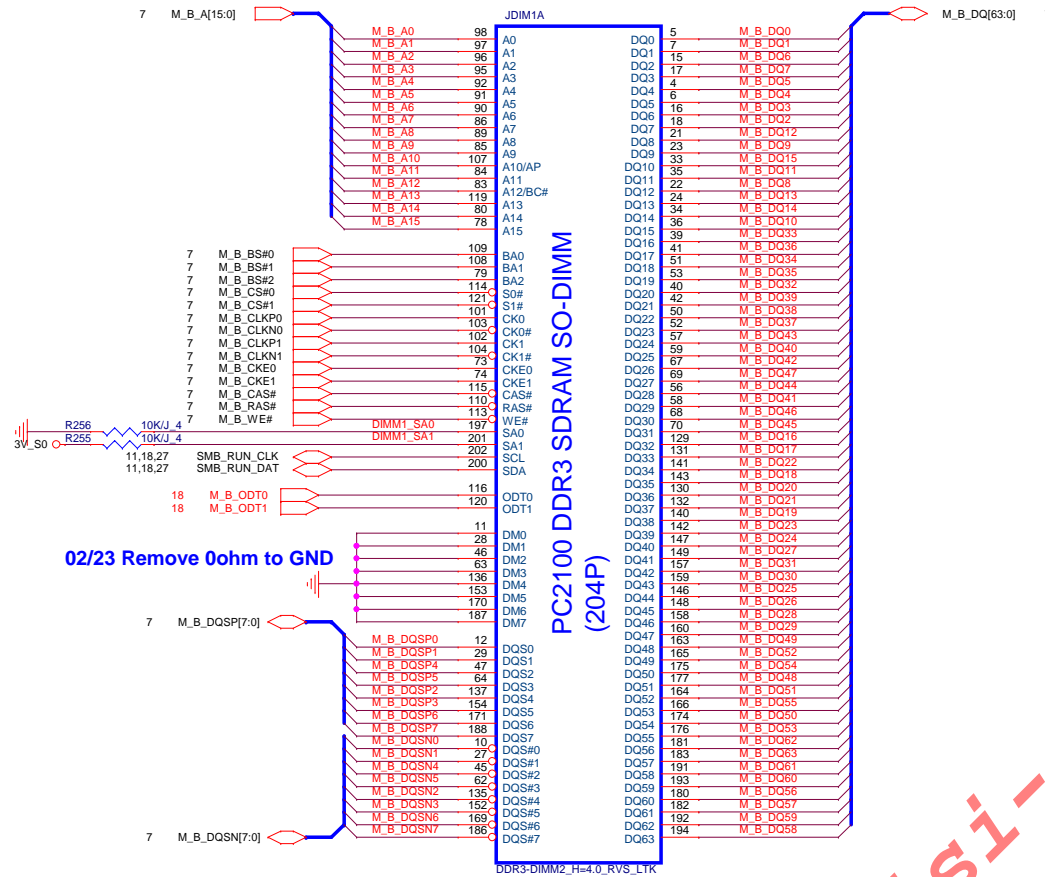
Place these Caps near So-Dimm0.



VREF DQ0 M1/M3 Solution

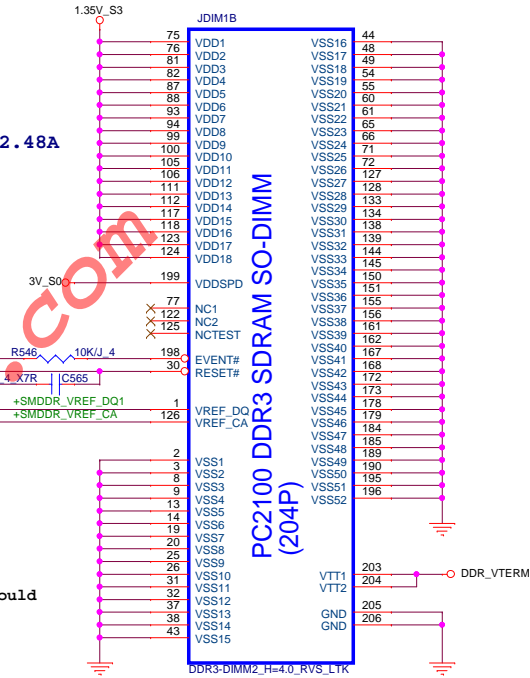


DDR_RVS (DDR)

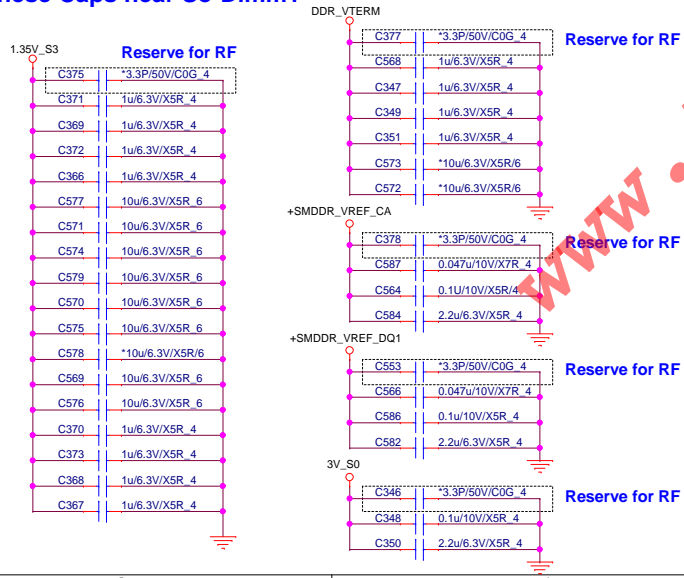


CAD Note: All VREF traces should have 10 mil trace width

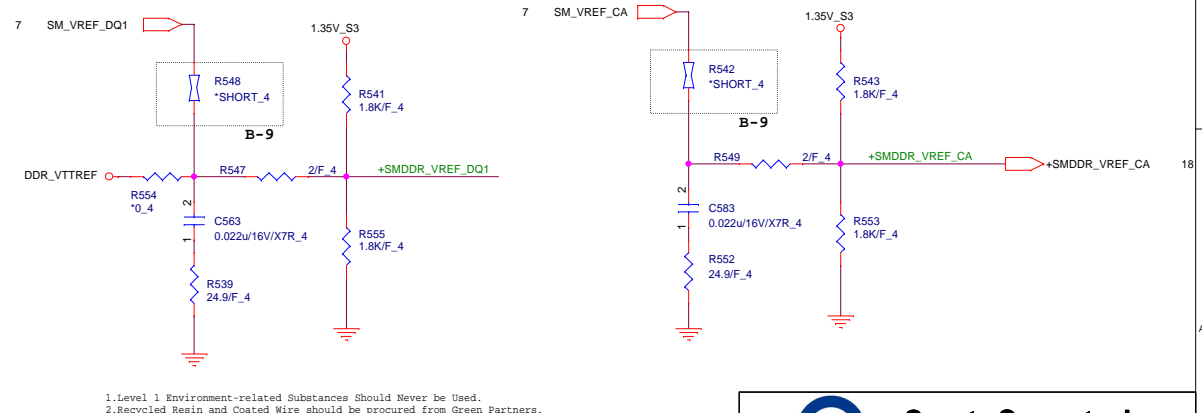
2.48A



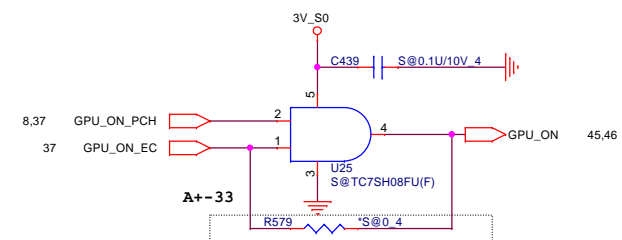
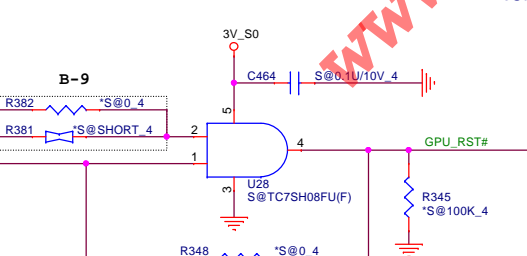
Place these Caps near So-Dimm1

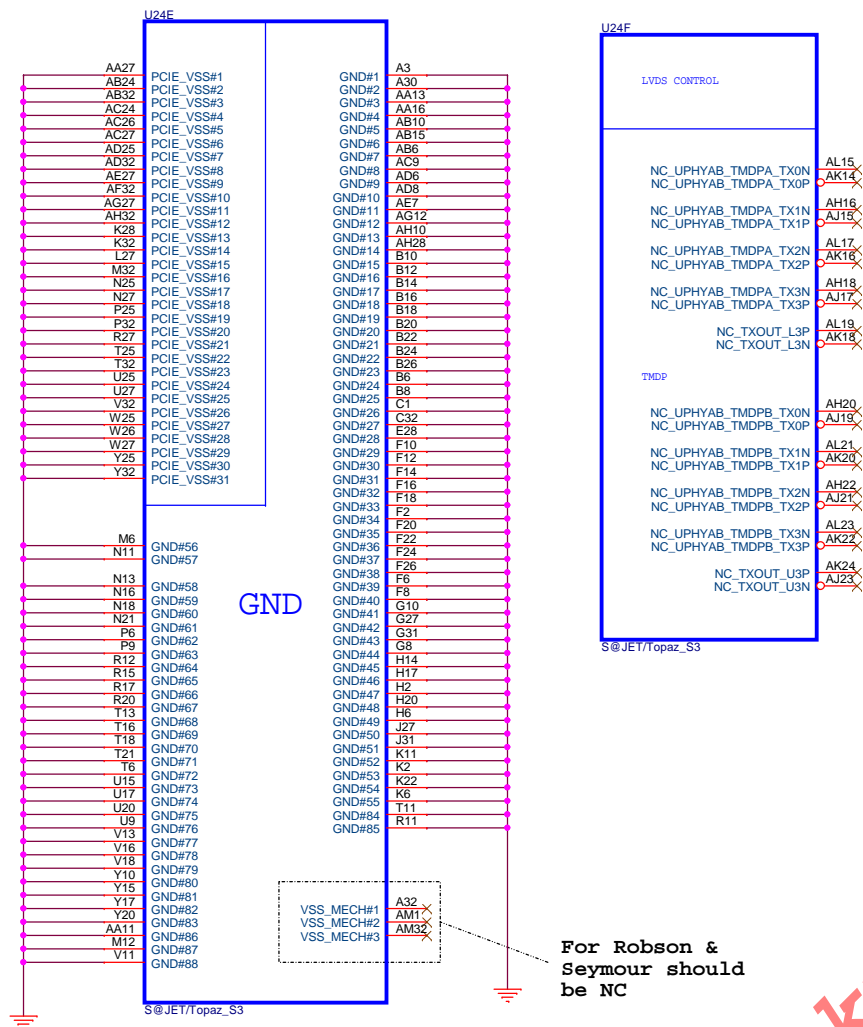


VREF DQ1 Solution



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.





CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1= INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/W/histler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYN	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

Memory Aperture size

GPIO_9 BIOSROM		GPIO_13 ROMIDCFG2	GPIO_12 ROMIDCFG1	GPIO_11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	Reserved	0	1	1
0	512M	Not Supported		
0	1G	Not Supported		
0	2G	Not Supported		
0	4G	Not Supported		

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

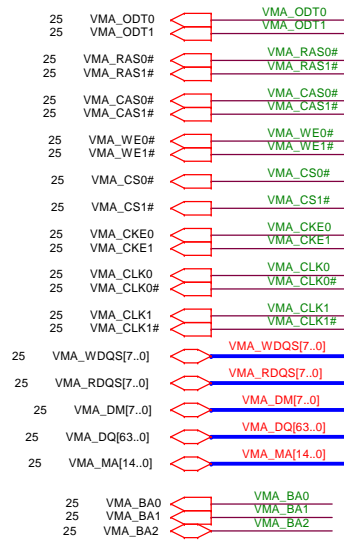


Quanta Computer Inc.

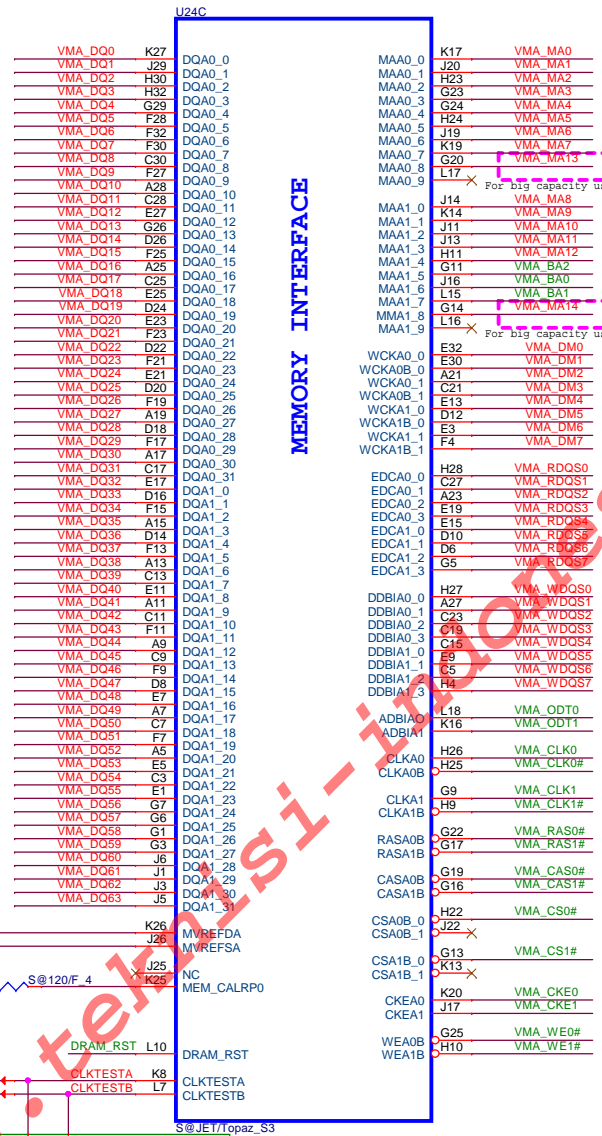
PROJECT : FH9

Size	Document Number	Rev
	JET/TOPAZ_S3_GND/LVDS/Strap	2A
Date:	Wednesday, November 19, 2014	Sheet 22 of 48

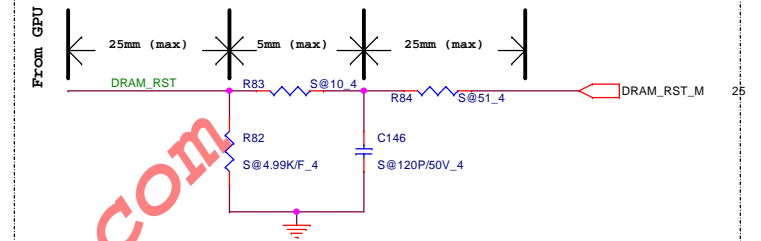




support 1Gbit
VRAM (64M X 16)

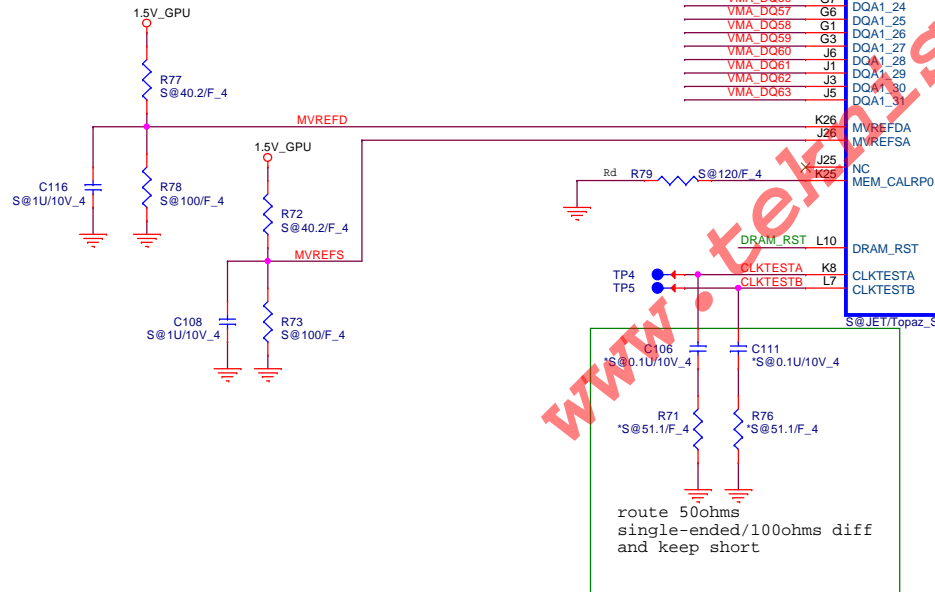


MEMORY INTERFACE



Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

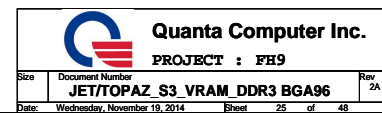


route 50ohms
single-ended/100ohms diff
and keep short



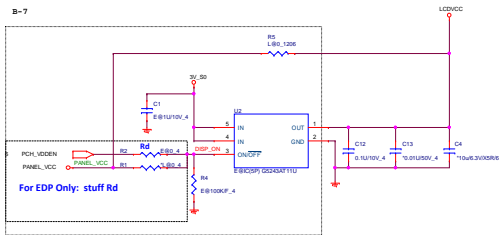
Quanta Computer Inc.

PROJECT : FH9

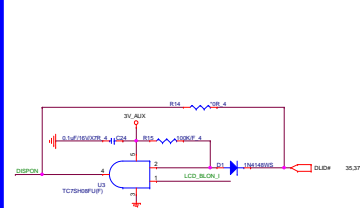


LCD POWER SWITCH

B-7

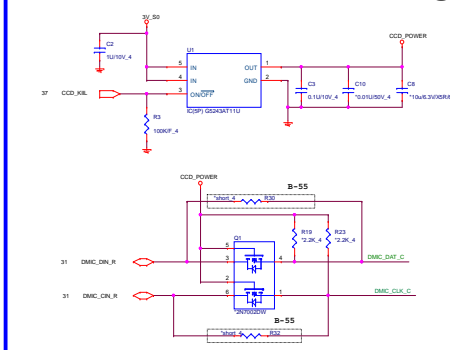


PANEL BACKLIGHT CONTROL



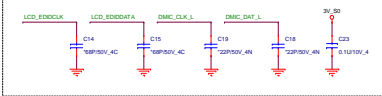
CCD KILL

28

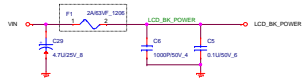


LCD CONNECTOR

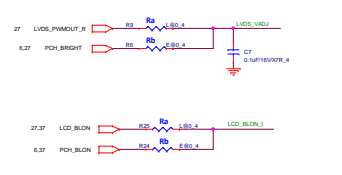
For EMI close to connector



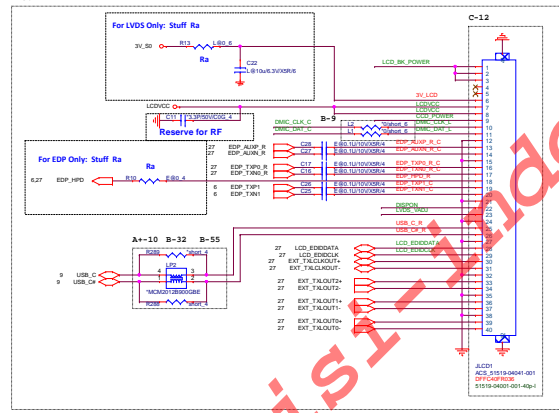
C-24



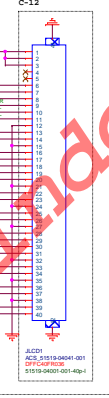
For LVDS Only: stuff Ra
For EDP Only: stuff Rb



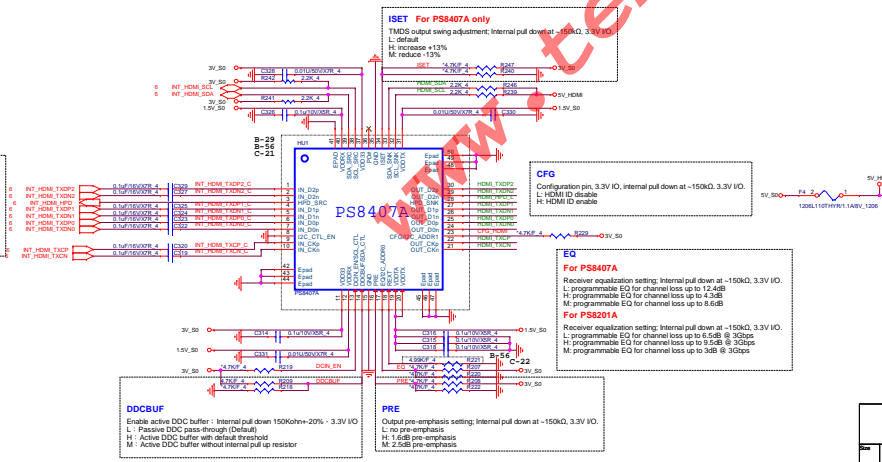
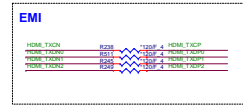
B-36



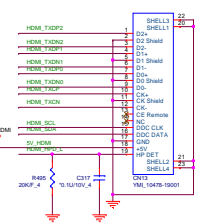
C-12

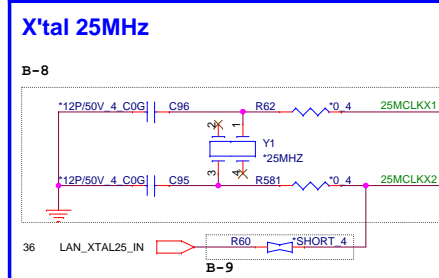
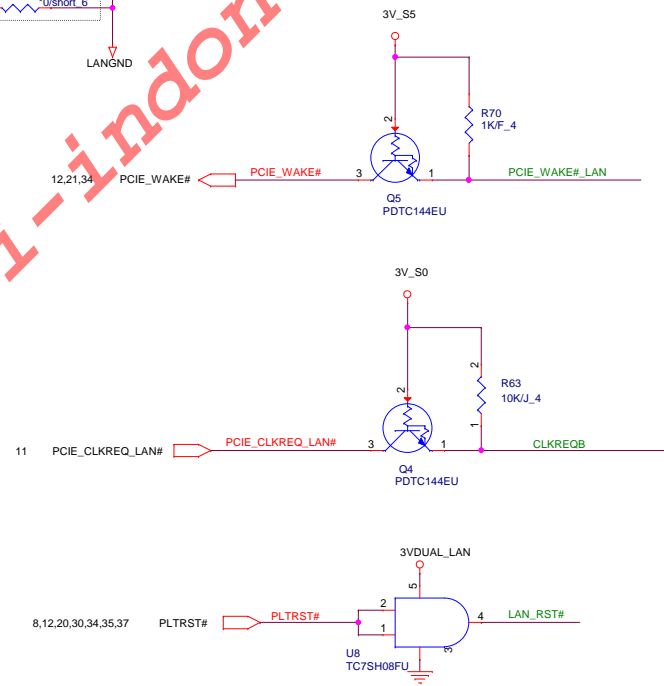
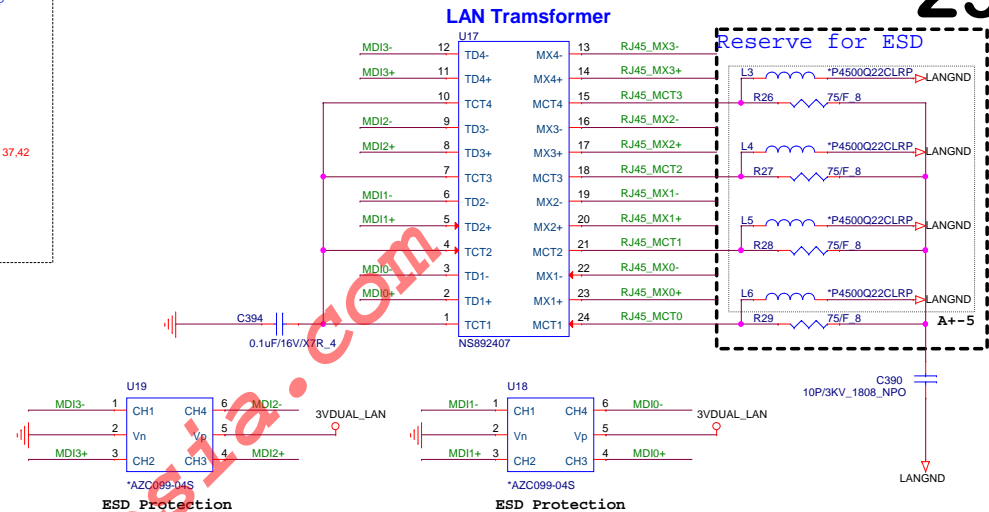


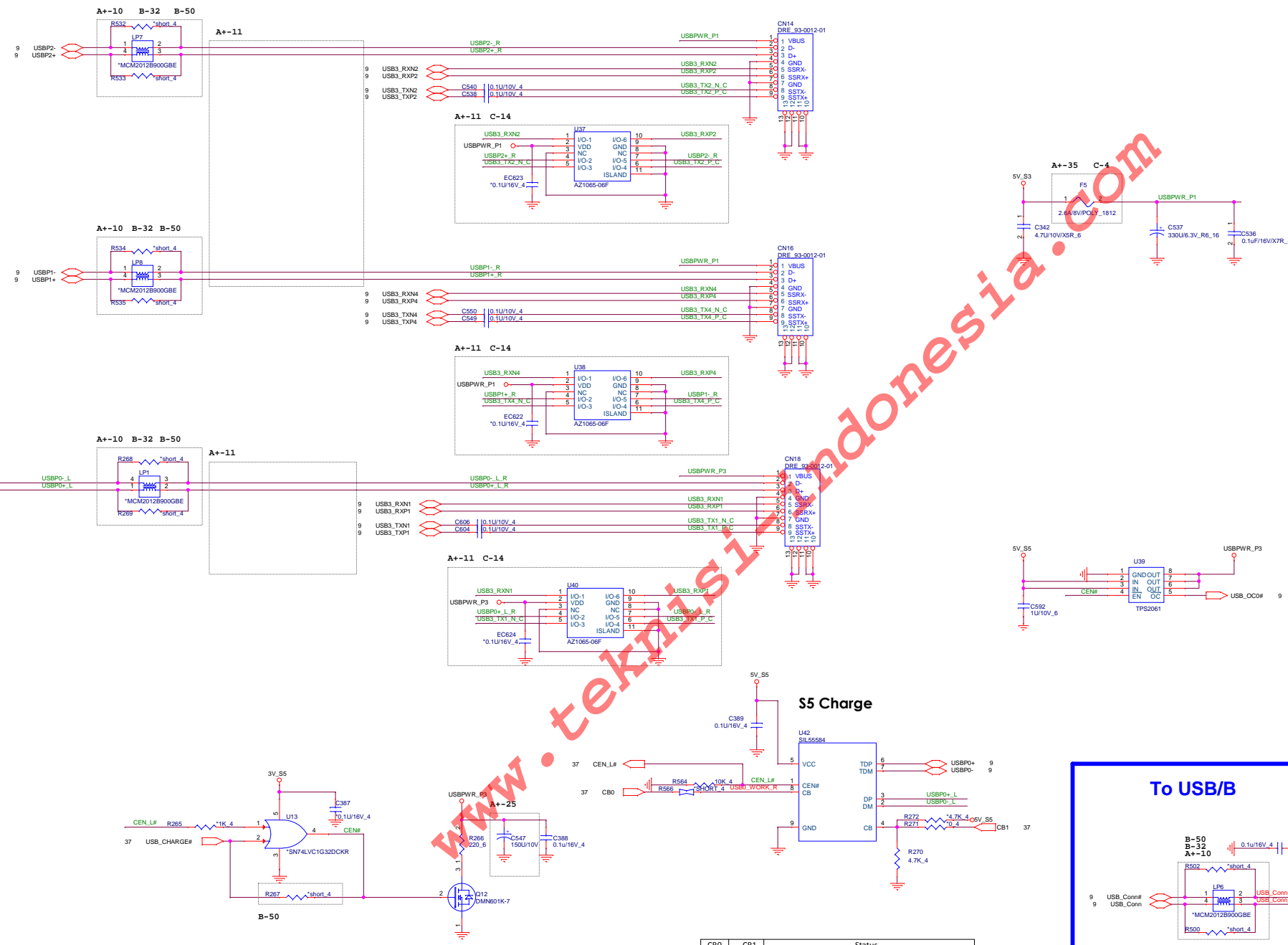
HDMI



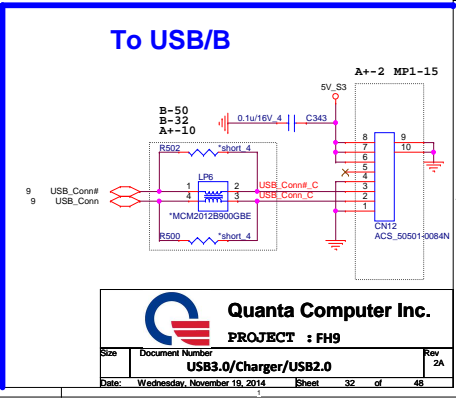
HDMI PORT



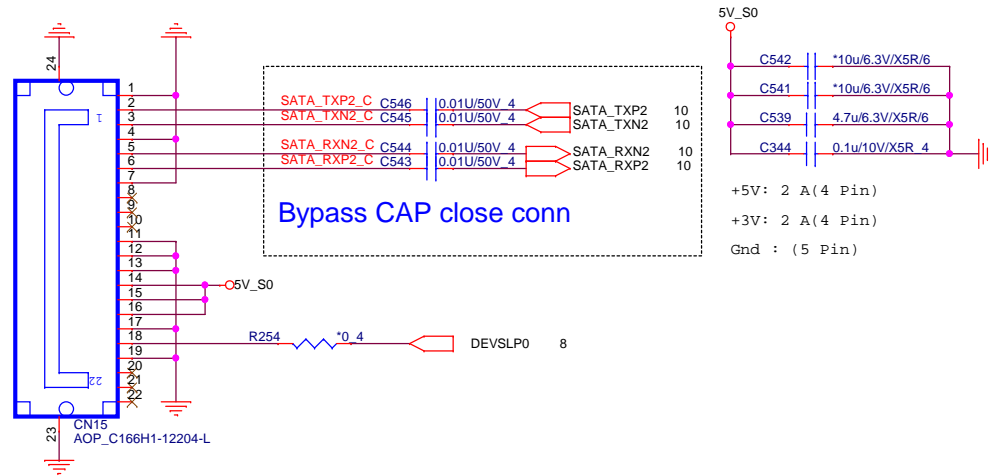




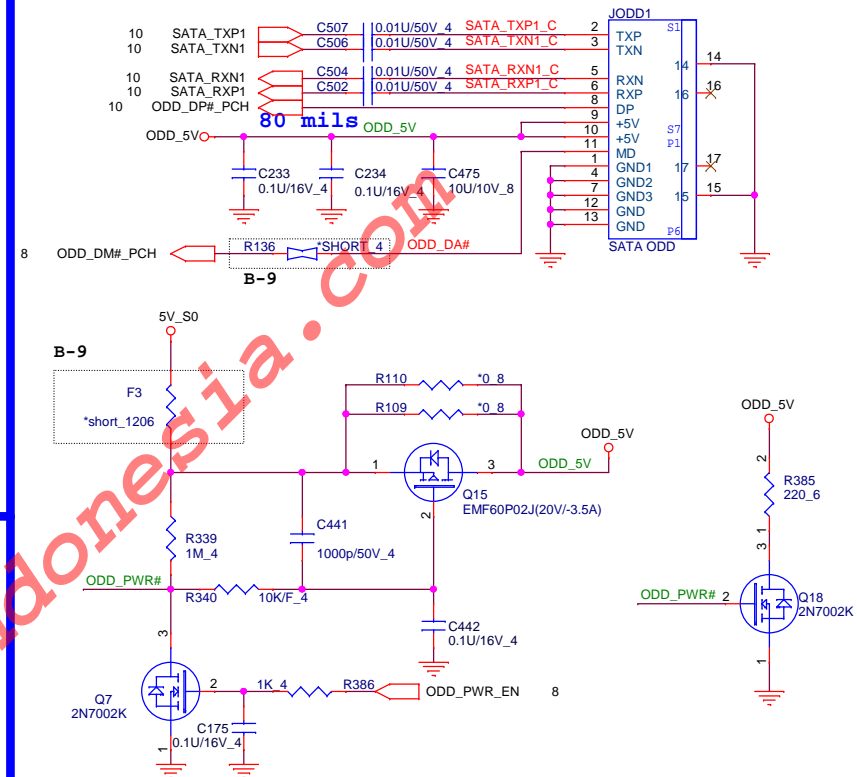
CB0 CB1		Status
0	0	Auto Dection Charge Mode
0	1	Force Dedicated Charger Mode
1	0	Pass Through Mode
1	1	Pass Through Mode with CDP or SDP(SIG5584 only)



SATA HDD Connector



SATA ODD Connector



LED

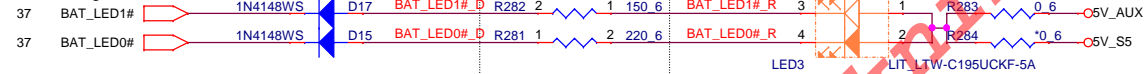
CAPS LED



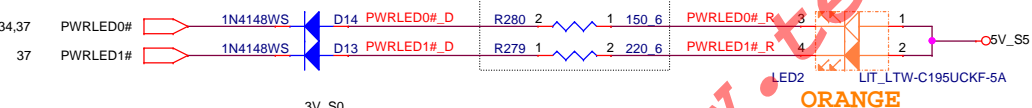
WLAN



Battery



Power Status



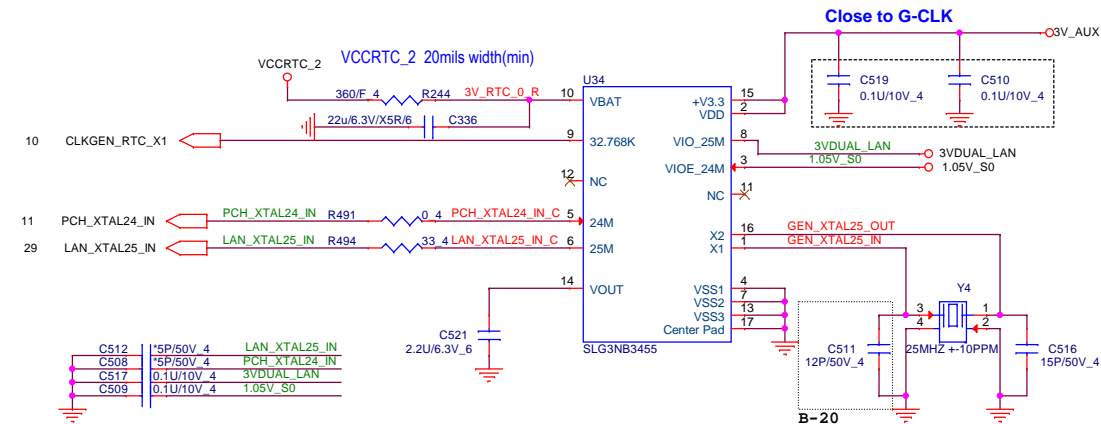
HDD/ODD



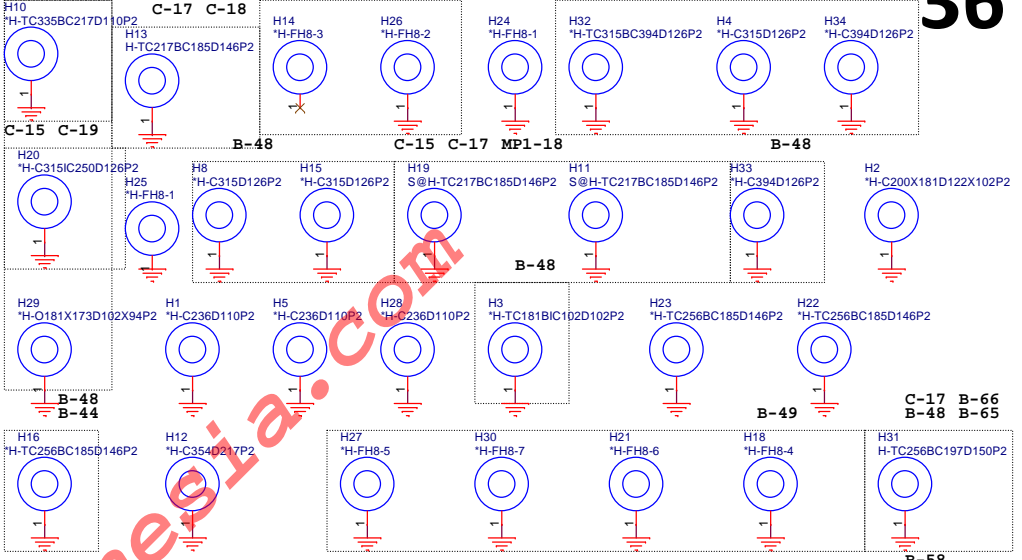
NUM LED



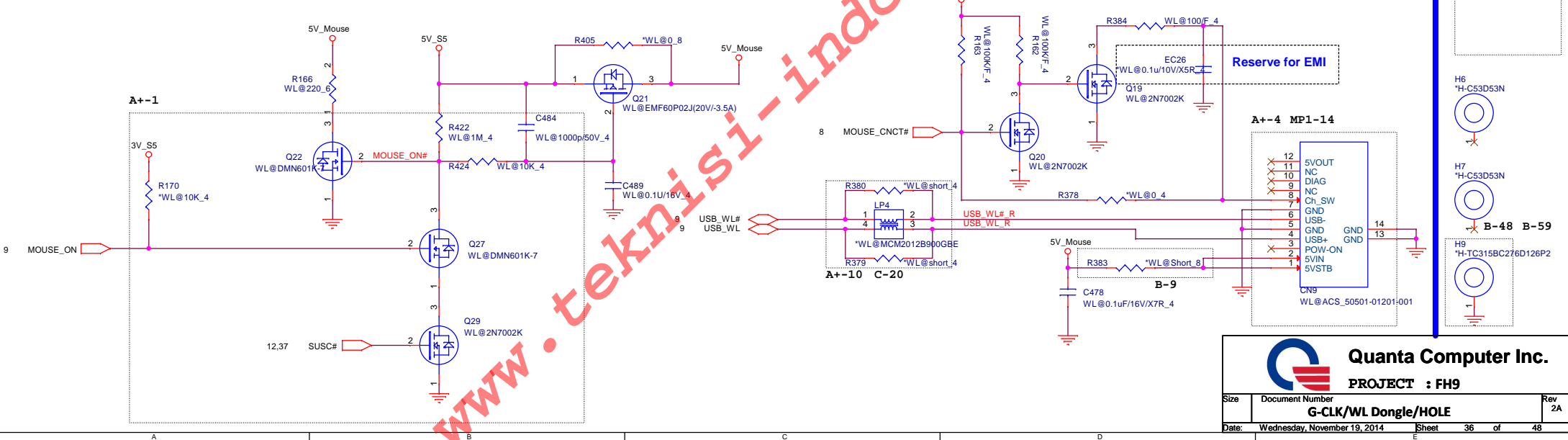
Green CLK Circuitry



HOLE

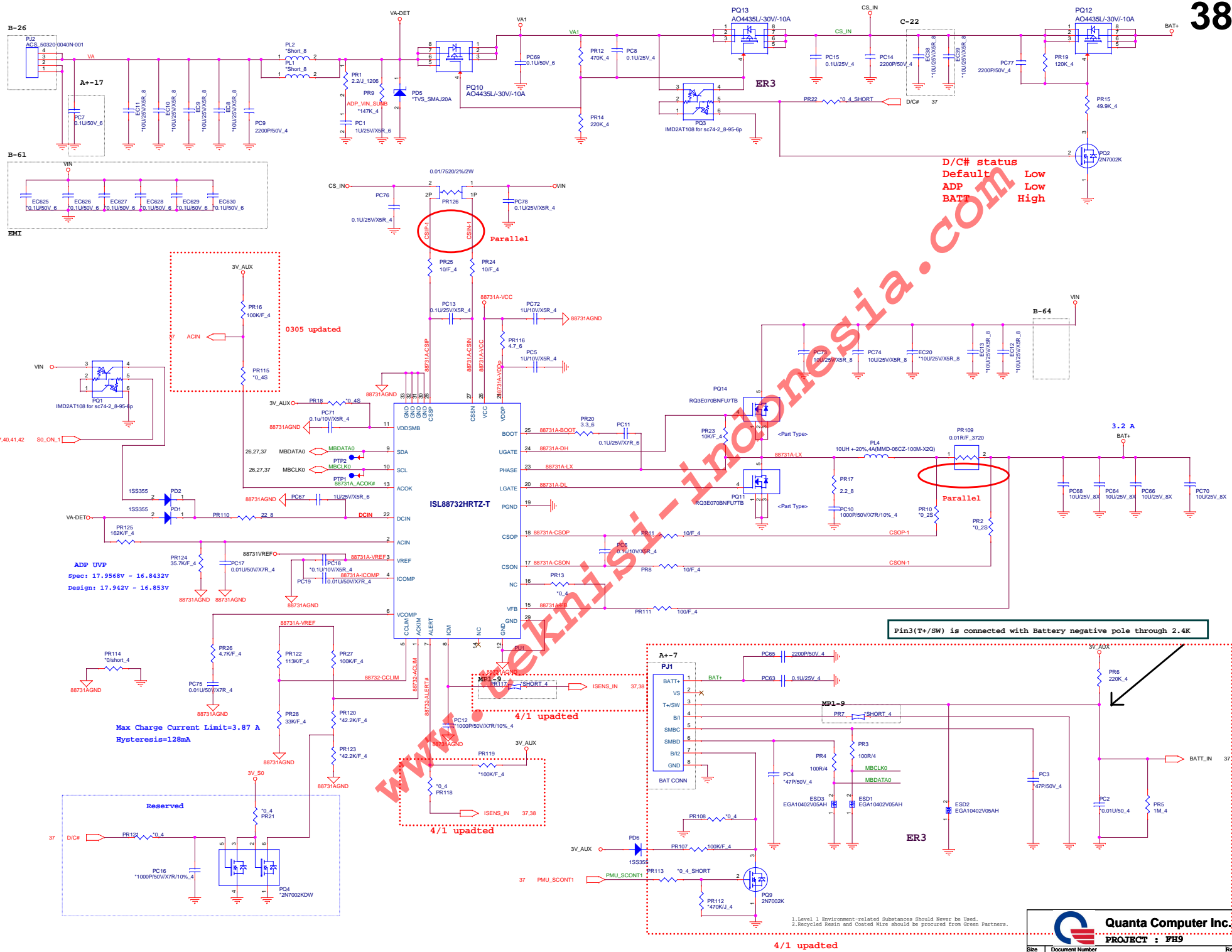


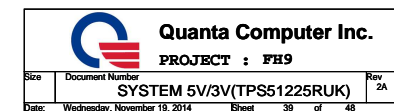
Wireless Dongle



Quanta Computer Inc.
PROJECT : FH9

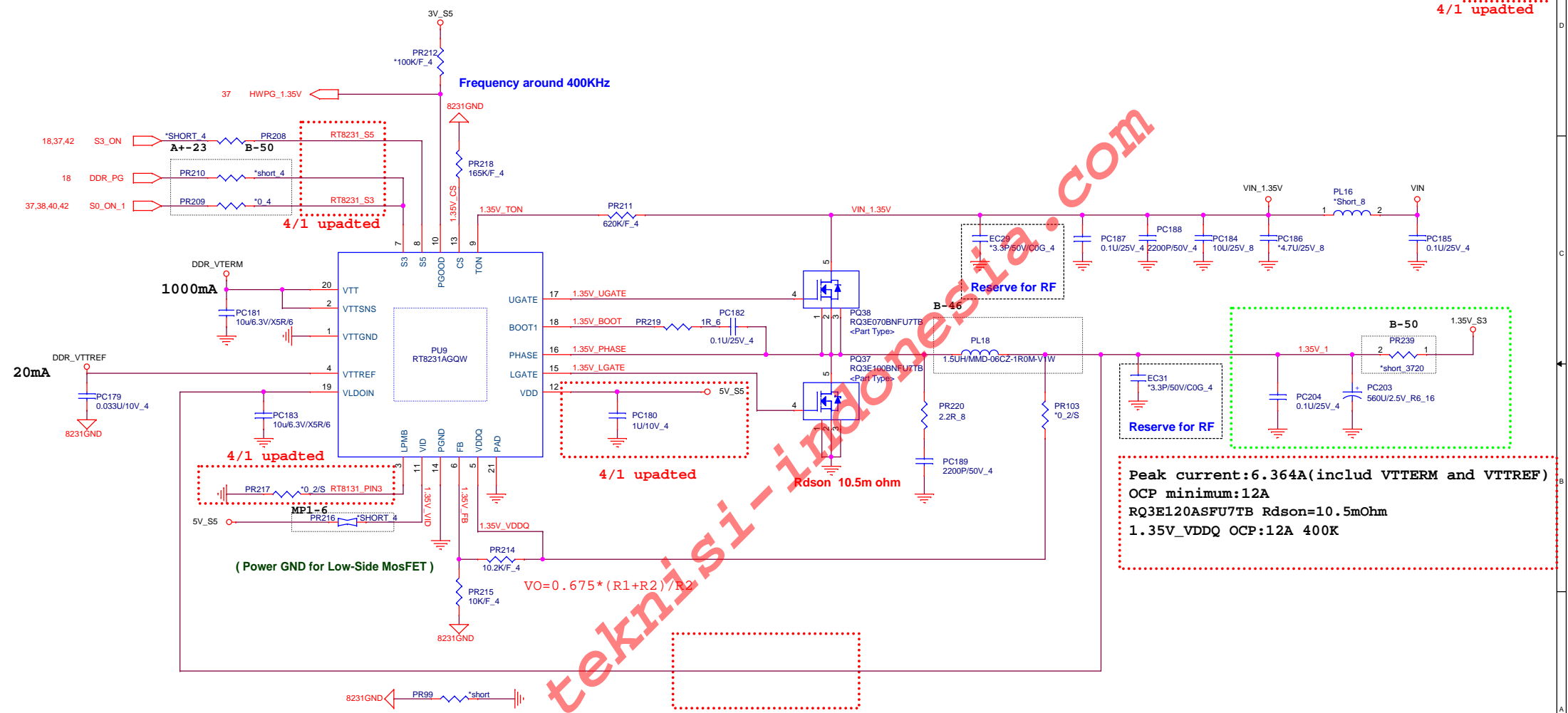
Size	Document Number	Rev
	G-CLK/WL Dongle/HOLE	2A
Date	Wednesday, November 19, 2014	Sheet 36 of 48





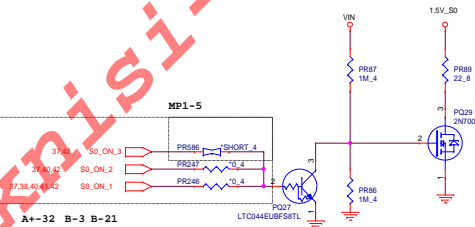
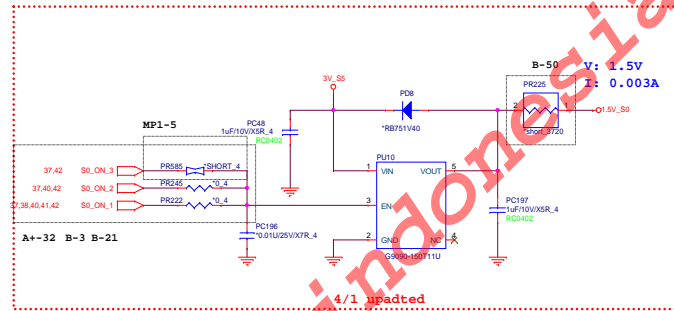
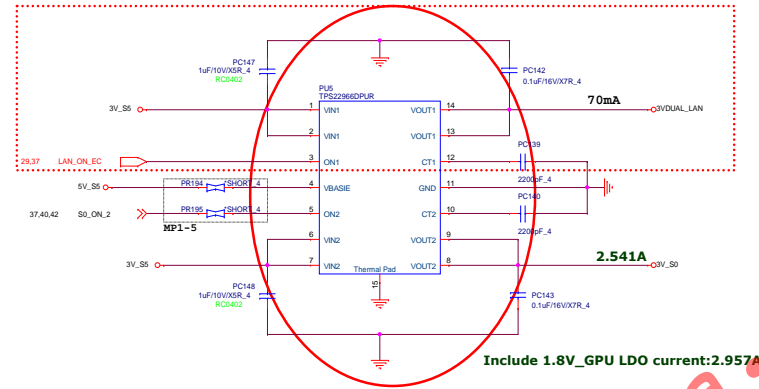
1.35V_VDDQ(RT8231AGQW)

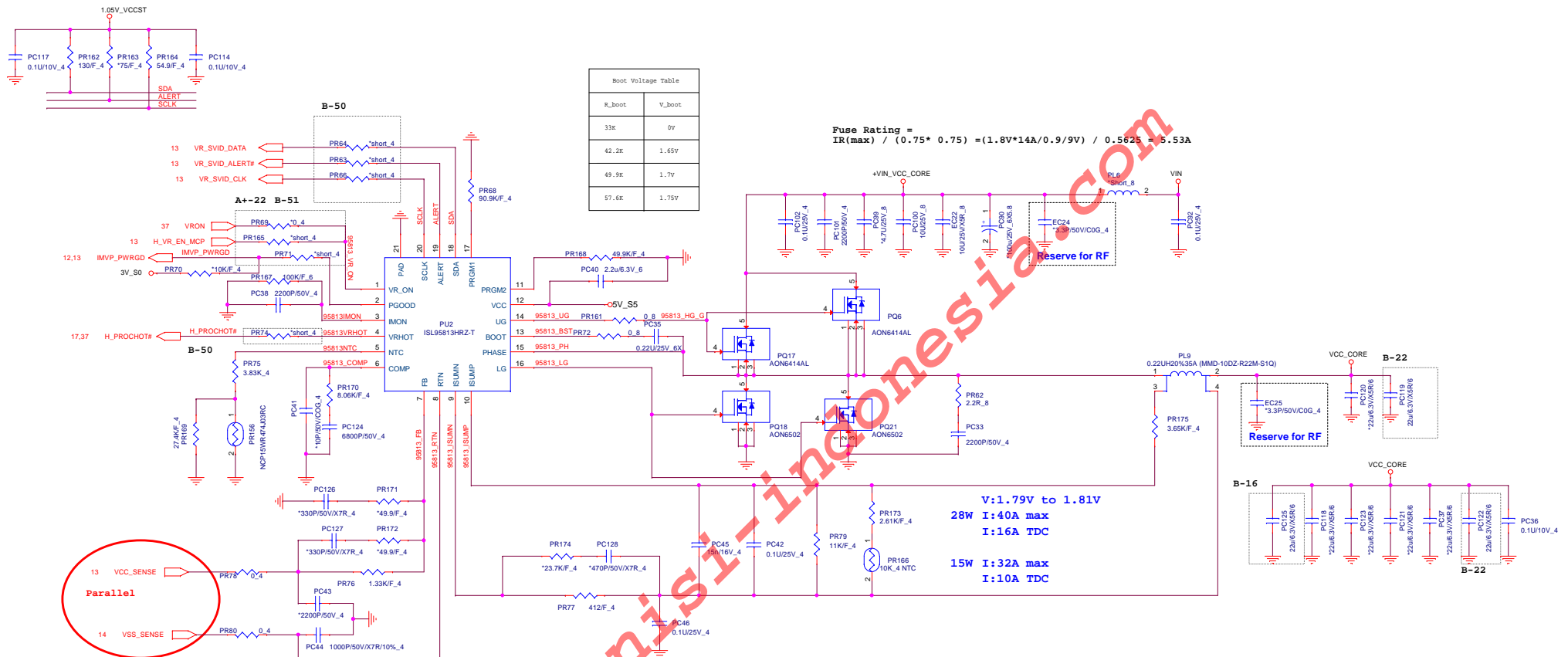
4/1 upadted



Peak current:6.364A(includ VTTERM and VTTREF)
OCP minimum:12A
RQ3E120ASFU7TB Rdson=10.5mOhm
1.35V_VDDQ OCP:12A 400K

04/14 updated No footprint





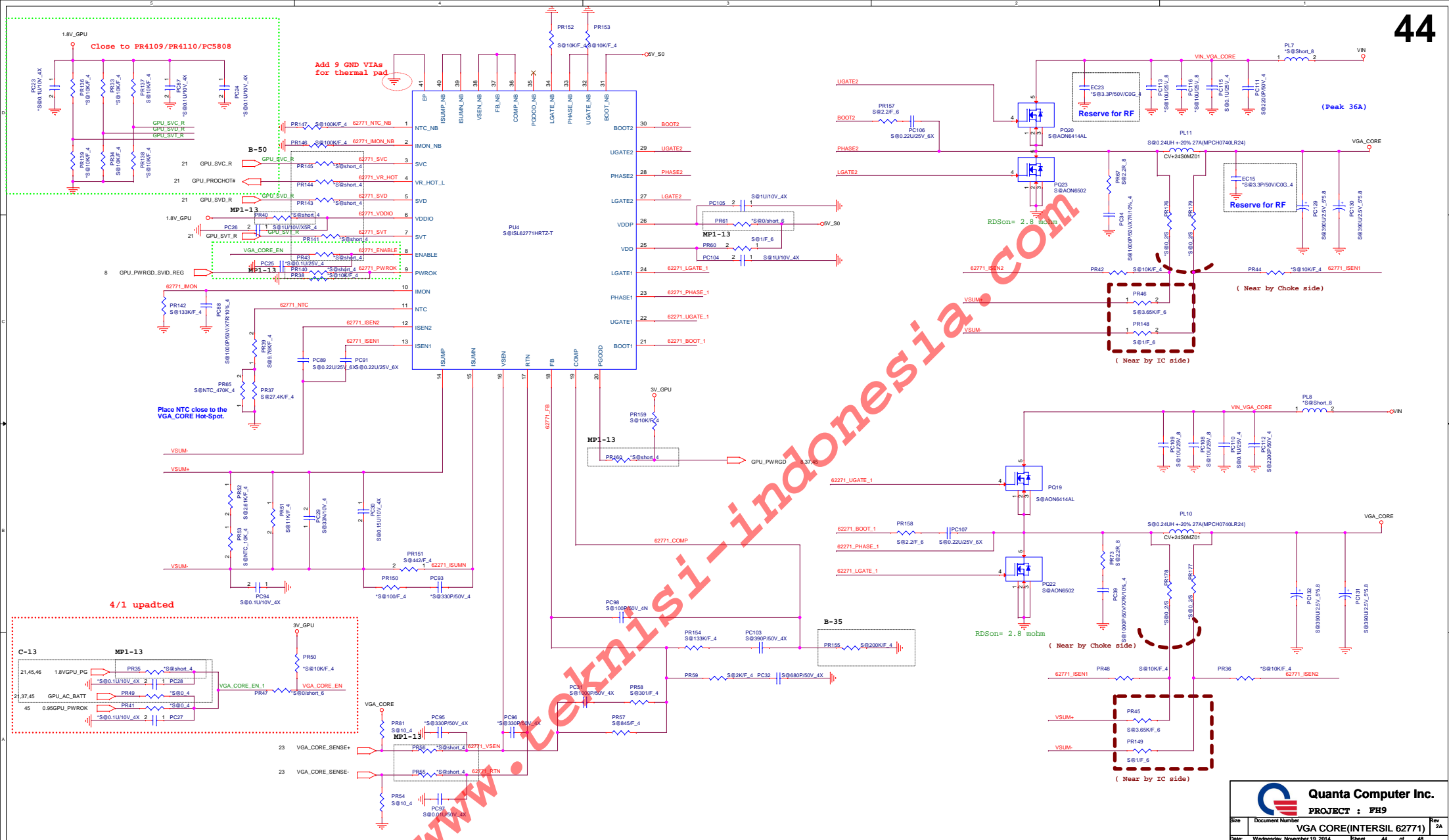
		28W	15W
B-41	(Iccmax)	PR68 113K(CS41132FB17)	90.9K(CS39092FB11)
	(IMON)	PR167 105K(CS41053F919)	100K(CS41003F932)
	(Loadline)	PR76 1.65K(CS21652FB29)	1.33K(CS21332FB11)
	(OCP)	PR77 510(CS15102FB19)	412(CS14122FB15)

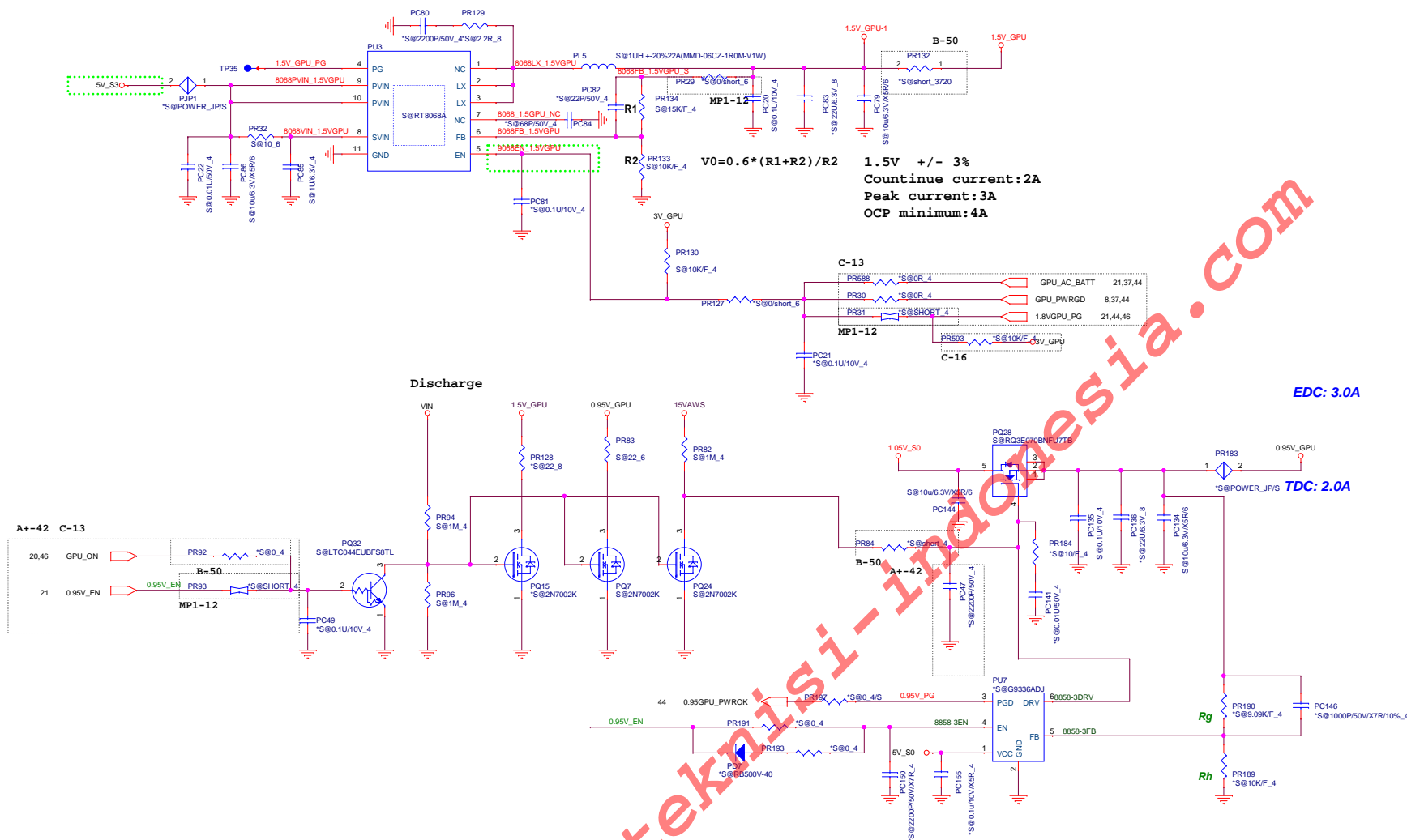


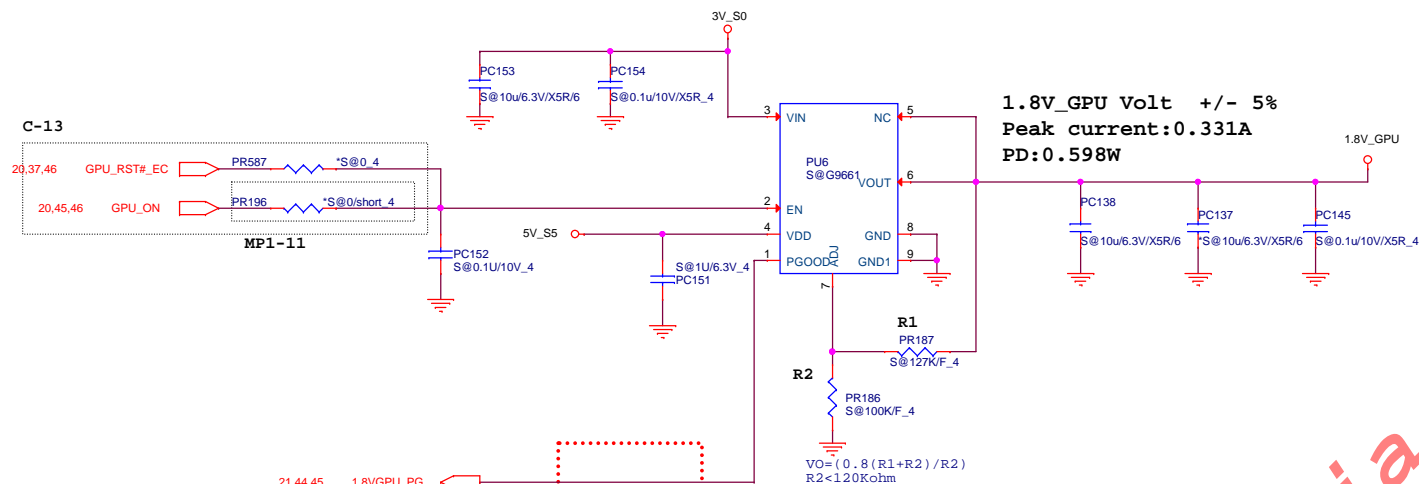
Quanta Computer Inc.
PROJECT : FB9

Size Document Number
CPU Core (ISL95813HRZ)JUL
Date: Wednesday, November 19, 2014 Sheet 43 of 48

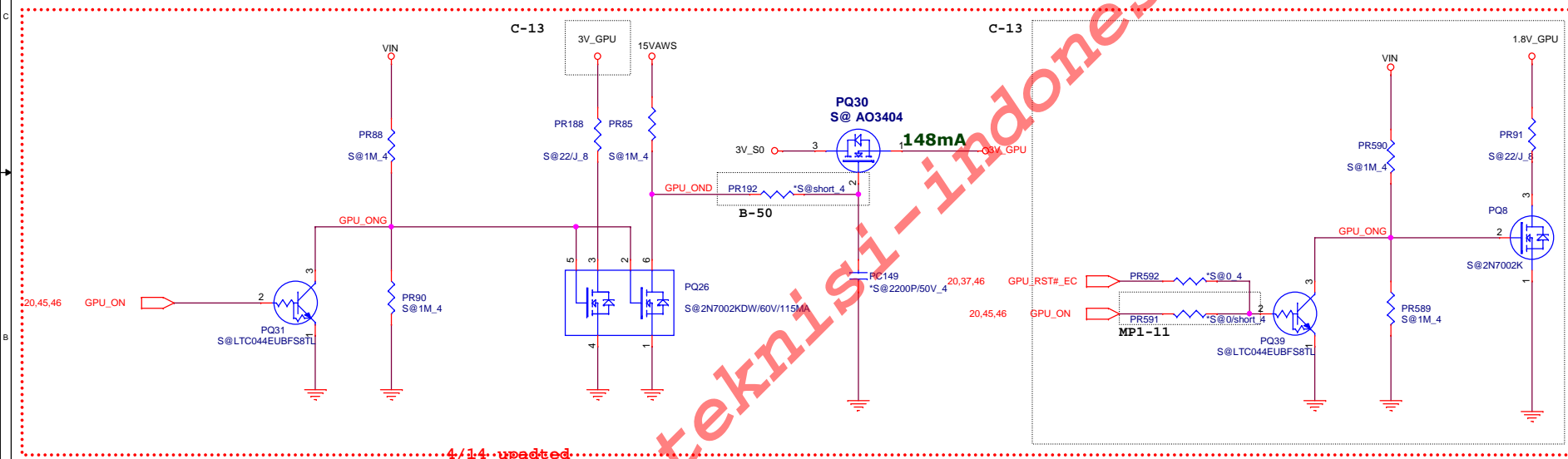
1. Level 1 Environment-related Substances Should Never be Used.
2. Recycled Resin and Coated Wire should be procured from Green Partners.







4/1 upadted



Quanta Computer Inc.

PROJECT : FH9

Size	Document Number	1.8V_GPU&3V_GPU	Rev 2A
Date:	Wednesday, November 19, 2014	Sheet 46 of 48	



Item	Stage	Page	Owner	Change explanation
13	R-PC	44,45,46	RE	for reserve RC control GPU power sequencer: P851 change to toba un-stuff, P853 change to toba stuff. P856 change to toba stuff, reserve P857 for GPU.B7F8 RC control, add dis-charge RCN for optim. P851 change to toba and reserve P858 for GPU.AC.BATT control 1.3V.DPU. P853 change to toba stuff, VGA_CORE reserve control 0.9V.RM change to GPU.AC.BATT.
14	R-PC	33	ME	Change P13 P/F to B-31A1C25014922for RSD request
15	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
16	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
17	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
18	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
19	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
20	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
21	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
22	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
23	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
24	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
25	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
26	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
27	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
28	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
29	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
30	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
31	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
32	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
33	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
34	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
35	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
36	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
37	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
38	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
39	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
40	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
41	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
42	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
43	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
44	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
45	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
46	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
47	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
48	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
49	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
50	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
51	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
52	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
53	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
54	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
55	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
56	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
57	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
58	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
59	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
60	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
61	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
62	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
63	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
64	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
65	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
66	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
67	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
68	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
69	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
70	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
71	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
72	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
73	R-PC	36	ME	Change P13 P/F to B-31A1C25014922for RSD request
74	R-PC	36	ME	